Accurate measurement of electrical bulk resistivity and surface leakage of CdZnTe radiation detector crystals

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A classical method for the accurate measurement of the bulk resistivity and a quantitative separation of bulk and surface leakage currents in semi-insulating CdZnTe radiation detectors is evaluated. We performed an extensive set of experiments on CdZnTe single-crystal test devices to confirm the reliability and reproducibility of the measurements and the validity of the underlying assumptions for data analysis and parameter extraction. The experiments included temperature dependent dual current-voltage measurements on devices with guard electrodes as a function of device thickness, surface preparation, surface passivation, and electrode deposition conditions. We also evaluated the temperature dependence of the bulk resistivity and implemented a general temperature normalization routine to allow a reliable comparison between various crystal samples. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2209192]

I. INTRODUCTION

The high atomic number of its components, large density, nearly ideal band gap, and relatively good charge transport properties make CdZnTe an attractive material for room-temperature (RT) x-ray and gamma-ray detector applications.[1] Progress in the electrical compensation and crystal growth techniques in recent years[2] made this technology commercially available for numerous x-ray and gamma-ray imaging and spectroscopy applications. Despite significant efforts the mechanism of electrical compensation and the underlying defect structure producing semi-insulating CdZnTe crystals with good charge transport properties is not yet fully understood.[3] Accurate experimental bulk resistivity data are essential to examine the applicability and performance of sophisticated compensation models and experimental techniques aimed at producing semi-insulating CdZnTe. In addition, bulk resistivity is a useful physical property in order to study the macro- and microsegregation of electrically active defects in CdZnTe. Reliable surface resistance measurements are critical to investigate the influence of various surface preparation and passivation methods on the surface leakage of CdZnTe radiation detectors.

Although electrical bulk resistivity, surface resistance, and leakage current are conceptually simple physical properties, their measurement in semi-insulating materials is not necessarily trivial. Particularly, in the literature of CdZnTe x-ray and gamma-ray detector devices, the simple but very important roles of Schottky barriers, temperature variations, and surface conductance are repeatedly overlooked or ignored, which can produce erroneous bulk resistivity and majority carrier-type data.

In this contribution we critically review bulk resistivity and surface resistance measurement techniques for semi-insulating CdZnTe single crystals and provide a comprehensive analysis of the various error sources. We also provide a very accurate method of reliably measuring the CdZnTe bulk resistivity and surface resistance based on the classical guarded two-probe technique. We also include a simple temperature normalization method that allows accurate comparison of bulk resistivity and surface resistance data acquired without controlled sample temperature. To demonstrate the power and accuracy of the experimental method we apply it to the measurement of the spatial distribution of the bulk resistivity along the growth axis of a CdZnTe ingot and to a series of surface processing and passivation experiments on CdZnTe detector devices.

II. BASIC CONSIDERATIONS

Using the material parameters as summarized in Table I,[4–8] the bulk resistivity of fully compensated $Cd_{1-x}Zn_xTe$ with 10% Zn ($x=0.1$) can be estimated to be about 4×10^{10} Ω cm at 296 K. This is the simplest possible

TABLE I. CdTe and CdZnTe material parameters.

RT electron drift mobility $Cd_{0.9}Zn_{0.1}Te$ ($cm^2/V\,s$)	1000	4
RT hole drift mobility $Cd_{0.9}Zn_{0.1}Te$ ($cm^2/V\,s$)	50	4
Electron effective mass CdTe (0.91×10^{-30} kg)	0.11	5
Hole effective mass CdTe (0.91×10^{-30} kg)	0.73	6
E_0 (eV)	1.606	7
a_1 (eV)	0.38	adjusted
a_2 (eV)	0.463	7
a_3 (eV/K)	4.5×10^{-4}	adjusted
a_4 (K)	264	8

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estimate, because in the ideal case of full compensation ($n \cong p \cong n_i$), the bulk resistivity ρ_i is given by

$$\rho_i = \frac{1}{q n_i (\mu_n + \mu_p)}, \tag{1}$$

where q is the elementary charge and μ_n and μ_p are the drift mobilities of the electrons and holes, which are generally composition and temperature dependent and n and p are the equilibrium concentrations of free electrons and holes. The intrinsic carrier concentration n_i is per definition,

$$n_i = \sqrt{4\left(\frac{2\pi k_B T}{h^2}\right)^3 (m_e^* m_h^*)^{3/2} \exp\left(\frac{-E_g}{k_B T}\right)}, \tag{2}$$

where m_e^* and m_h^* are the (actually, composition dependent) electron and hole effective masses and h and k_B are the Planck's and Boltzmann's constants. The band gap energy E_g depends on the temperature T and on the composition x. We are using the following formula to generate an approximate $E_g(T,x)$ matrix,

$$E_g = E_0 + a_1 x + a_2 x^2 - \frac{a_3 T^2}{a_4 + T}. \tag{3}$$

The used parameters E_0 and $a_1 - a_4$ are also listed in Table I. Some of them are taken from published experimental data[7,8] and some have been arbitrarily adjusted to match established low- and room-temperature band gap data of purely binary CdTe and ZnTe.

Note that fully compensated ($n \cong p$) material would still behave n type in a thermoelectric current experiment since the drift mobility of the electrons is much larger than the mobility of the holes ($\mu_n > \mu_p$). An even higher resistivity than the intrinsic one can be obtained for p-type material ($p > n$) with a maximum at $\mu_p p = \mu_n n$. Furthermore, CdZnTe ingots grown from the melt by directional solidification (Bridgman, gradient freeze, and electrodynamic gradient freeze) show a significant Zn segregation so that the nominal Zn concentration is only obtained at a certain axial position. This affects the band gap and hence, the above estimate for the intrinsic resistivity ρ_i by almost a factor of 2 from tip to heel of a typical 10 cm long ingot.

In reality, the stable high-resistivity material is obtained by (generally incomplete) deep level compensation and the description of actual tip-to-heel resistivity profiles requires a rather careful analysis and modeling. Uncompensated high-purity CdZnTe, grown without partial pressure control, is typically low resistivity p type due to the dominance of acceptor defects in the crystals[3] and the concentration of the majority carriers may be saturated over a wide temperature range. In semi-insulating semiconductors, however, the temperature dependence of the carrier concentrations is always strong, which is important to keep in mind. Varying the temperature within a ±5 K window around room temperature can already cause a factor of 3 change in the bulk resistivity of semi-insulating (SI) CdZnTe crystals. In addition, surfaces typically have different electrical properties from the bulk material, i.e., their influence has to be experimentally separated or eliminated. Leaking surfaces are, in general, more detrimental the higher the bulk resistivity is and the surface resistivity may change with time and also in dependence on environmental conditions if no further passivation and/or coating is applied to the surface of the detector crystal.

Contactless methods aside (e.g., Ref. 9), the electrical properties of semiconductor crystals are measured by fabricating test devices with appropriate electrode materials and configuration. For semi-insulating CdZnTe crystals typically Pt, Au, In, or other metal electrodes are deposited by sputtering, evaporation, or electroless methods to form the test devices. The difference between the metal work function and the electron affinity of the CdZnTe crystal inevitably leads to the formation of a Schottky barrier at the metal-CdZnTe interface and a corresponding built-in potential in the CdZnTe crystal. The latter also depends on the semiconductor's Fermi level position. The actual barrier heights are further influenced by surface energy states due to the disruption of the crystal lattice at the semiconductor surface, which makes them hard to predict *a priori*. Also, interfacial oxide layers may additionally blur the effect of a particular electrode metal work function or, depending on the process, even completely dominate the barrier properties.

Unfortunately, the existence of the Schottky barrier is frequently ignored in many published works, which provides a first source of erroneous bulk resistivity data.

A second error source arises from poorly controlled properties of the surfaces. Freshly cleaved or more commonly, chemically, mechanically, or chemomechanically prepared CdZnTe crystal surfaces are highly reactive and typically form films of lower resistivity than the bulk material unless adequate process steps are employed to form high-resistivity surface passivation films. Parallel conduction (and also thermoelectric-current generation) in the leaky low-resistance surface films have often been ignored in literature data.

Next, we will examine the influence of the Schottky barriers and surfaces on bulk resistivity measurements and present an effective and accurate method to minimize their effect on the experimental bulk resistivity data.

III. FOUR-PROBE METHOD AND SURFACE SHUNT

The method of choice to eliminate errors due to non-Ohmic contacts is the four-probe technique, in which a measurement current is driven through the semiconductor sample via one contact pair ($c1$ and $c2$) and the resulting potential difference V is measured on a separate contact pair ($c3$ and $c4$). This is illustrated in Fig. 1. Any voltage drop over non-ohmic contacts V_{c1} and V_{c2} only increases the compliance voltage the current stabilizer circuitry requires to drive the desired current I_m through the sample and does not, in principle, affect the measurement. The important requirement for the potential measurement device(s) is that the input resistance R_i has to be high enough, so that virtually no current flows in this circuit, i.e., no additional voltage drop over the contacts can occur $V_{c3} \approx V_{c4} \approx 0$. In the real setup, the potential measurements are typically not done with a single device but in a differential configuration in which separate buffer amplifiers are used to measure the potential differences between the contacts and ground and the difference between

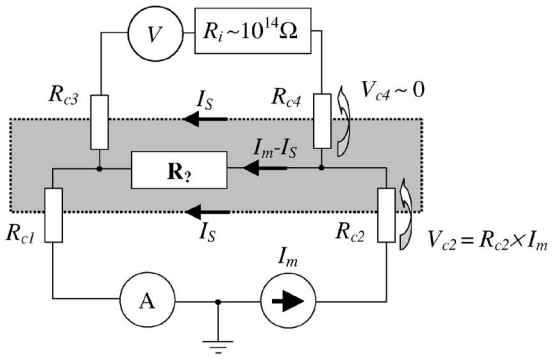

FIG. 1. Schematic illustration of a four-probe measurement and errors due to surface shunt.

the two amplifier output signals (low impedance) is measured with a conventional isolated multimeter. This avoids possible common mode errors due to the finite isolation resistance between the instrument's LO terminal and chassis ground.[10]

This method, however, can be subject to significant errors due to parallel surface leakage currents. In this event, the actual bulk measurement current is reduced from its nominal value I_m by an unknown amount I_S and the measured potential differences will be smaller than those expected from the true bulk properties. The problematic surface current paths are indicated in Fig. 1. In practice, the entire surface of the crystal can contribute.

Even though, a proper surface passivation can reduce these effects to a certain degree, it will be in general difficult to eliminate them completely. For our high-resistivity CdZnTe ingots grown by the electrodynamic gradient freeze technique,[2] this usually resulted in significantly different (and always underestimated) bulk resistivity data ρ depending on the applied surface preparation and passivation technique. Also, the measured Hall coefficient R_H does not correctly reflect bulk properties and can, in extreme cases, even change its sign after modifying the surface of the same crystal sample.

Figure 2 shows an example of an actual surface modification experiment. Two CdZnTe single crystals from two different ingots were processed to the Van der Pauw configuration[11] and ρ and R_H were measured. Because of heavily leaking surfaces, none of the measured data reflect the actual bulk properties. After reetching the crystals in a

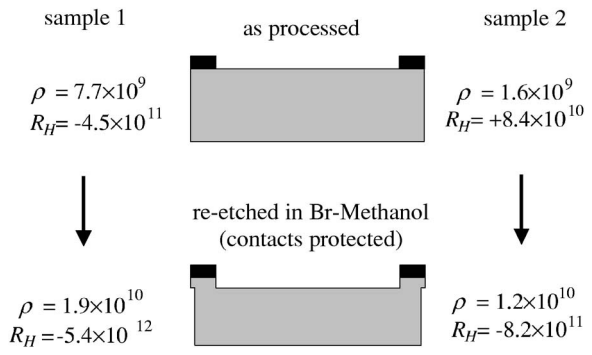

FIG. 2. Four probe results before and after surface modification (ρ and R_H values are in Ω cm and cm^3/C, respectively).

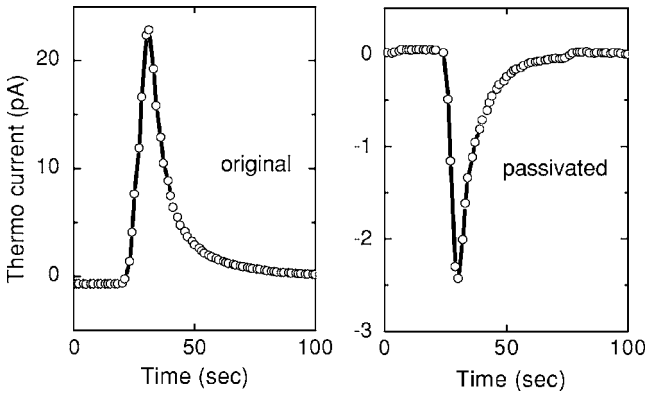

FIG. 3. Thermoelectric-current measurements before and after surface passivation. The peak corresponds to the time the heater was turned off.

bromine-methanol solution with the metal contact areas protected from the etching solution by an epoxy resin, the surfaces became less leaking but were still far from being properly passivated. The ρ and R_H data were dramatically different from the first measurement but still erroneous. In the case of sample 2, the measured Hall coefficient even changed its sign. Obviously, in this case, the surface leakage completely dominated the initial results and the extracted resistivity and Hall coefficient are not related to the bulk charge transport properties.

We sometimes observed similar sign changes in thermoelectric-current ("hot probe") experiments on parallel plate devices (single electrodes on two opposing surfaces of the crystals) after modifying or passivating the side surfaces. Note, that a sign change of the thermoelectric current in an ideal bulk measurement would occur at $\mu_p p = \mu_n n$ and the Hall coefficient changes its sign at $\mu_p^2 p = \mu_n^2 n$; hence, at a given temperature, only a change of the surface contribution can cause such a polarity change. Figure 3 shows the heating cycles (thermoelectric current versus time as the sample is heated) of hot probe measurements on the same CdZnTe crystal in the parallel plate electrode configuration before and after a passivation process has been applied to the side surfaces between the electrodes. In this example, the initial positive thermoelectric current was about one order of magnitude larger than the negative signal under similar heating cycle conditions after a high-resistivity surface passivation film has been generated.

IV. TWO-PROBE APPROACH

A classic approach to handle surface shunt leakage currents is a guarded current-voltage (I-V) measurement in which a bias voltage V_B is applied between two electrodes and the resulting current I is measured. In this configuration (Fig. 4) the surface leakage current does not contribute to the bulk current measured through the center electrode and can be separated from the total guard current once the true bulk resistivity is obtained from the measurement on the center electrode.

The guarded current-voltage technique, employed for bulk material conductivity characterization, requires that the measured current is limited by the semiconductor bulk resis-

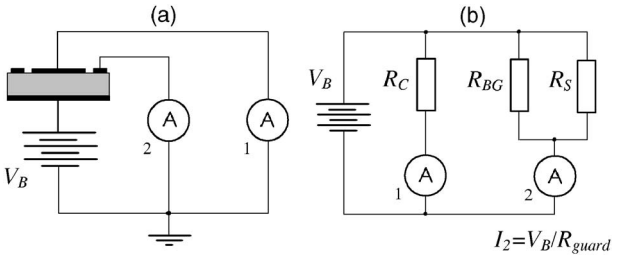

FIG. 4. Schematic illustration of a guarded two-probe measurement (a) and low-bias equivalent circuit (b).

tance. The ideal thermionic I-V_B characteristics of a Schottky diode with series resistance is given by (e.g., Ref. 12)

$$I = I_S\left\{\exp\left[\frac{q(V_B - IR_S)}{k_B T}\right] - 1\right\}, \tag{4}$$

where I_S is the reverse bias saturation current, q is the elementary charge, R_S is the series resistance of the semiconductor, k_B is the Boltzmann's constant, and T is the temperature. For small currents, one obtains for the series resistance,

$$R_S(I \to 0) = \frac{V_B}{I} - \frac{k_B T}{qI_S}, \tag{5}$$

where the second term can be considered as the zero-bias contact resistance R_C of the Schottky barrier. If the series resistance of the semiconductor is much higher than R_C, the second term in Eq. (5) gives only a negligible correction and R_S can be obtained directly from the I-V_B slope.

Consequently, this method is not easily applicable to low bulk resistivity material where the contact resistance can easily exceed the bulk resistance. For low resistivity material, a careful preparation of low resistance ("Ohmic") contacts is essential for accurate measurements.

In the case of high-resistivity material, however, a back-to-back Schottky barrier device will produce a linear, semiconductor dominated I-V curve in the voltage range where the current is limited by the series resistance of the bulk semiconductor and not by the reverse biased Schottky barrier. Such quasi-Ohmic behavior can be generally obtained if the bias voltage is small enough; the leakage current limited by the series resistance of the bulk semiconductor has to be much smaller than the saturation current of the reverse biased Schottky barrier. This range is schematically illustrated in Fig. 5 where we compare an ideal, series resistance-free thermionic current-voltage characteristics of two identical back-to-back Schottky barriers (full curve) with a pure Ohmic linear I-V curve of a bulk semiconductor (dashed line). When the bias voltage is much smaller than $\pm V_c$, the series resistance of the bulk semiconductor limits the leakage current and the bulk resistance can be determined from the fit of the linear I-V curve. It is clear from Fig. 5 that the series resistance controls the slope of the linear bulk semiconductor I-V curve and the value of V_c. The latter also depends on the majority carrier type as the reverse bias saturation current increases for p-type CdZnTe due to the higher hole effective mass (Table I), which enlarges the experimental window. For low resistivity bulk material the voltage range shrinks and the method becomes impractical at some point.

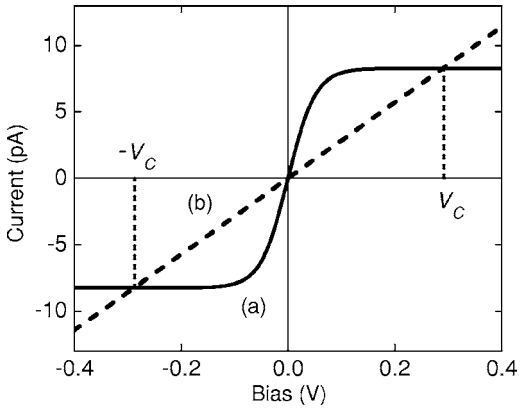

FIG. 5. Ideal thermionic current-voltage characteristics without series resistance (a) and bulk I-V curve (b).

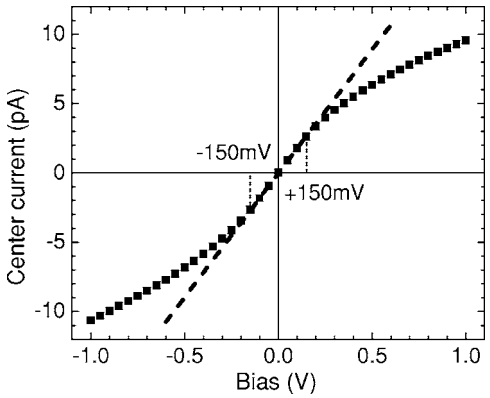

FIG. 6. Current-voltage characteristics measured on the guarded 5×5 mm^2 center electrode of a 2-mm-thick CdZnTe detector and linear fit in the bulk conductivity limited range (dashed line).

Another experimental limit of the technique, of course, is the requirement of an accurate measurement of very low currents with all the possible error sources typical for such low-level measurements (e.g., Ref. 10). Figure 6 shows an experimental I-V curve from the guarded center electrode of a CdZnTe detector in the voltage range between -1 and +1 V. In this particular case, the barrier influence becomes visible at voltages above ±150 mV. (A study of barrier and interface influenced high-bias I-V characteristics can be found in Ref. 13.)

In the following, we will outline a low-bias dual I-V method for guarded current-voltage measurements with all necessary corrections and normalizations to accurately measure bulk resistivity and surface resistance of semi-insulating CdZnTe and present experimental verification of the technique on detector-grade high-resistivity CdZnTe single crystals.

V. DUAL *I-V* SETUP AND LOW-BIAS SWEEP

The dual I-V measurements have been carried out using two Keithley 6517A electrometers and low-noise/low-capacitance Keithley 7024-3 triax cables outside the shielding enclosures (e.g., metal boxes or cryostat). Inside wiring was done with low-capacitance coax cables with the shield connected to the respective electrometer LO and open at the probe side. In all cases, the enclosure was grounded via the

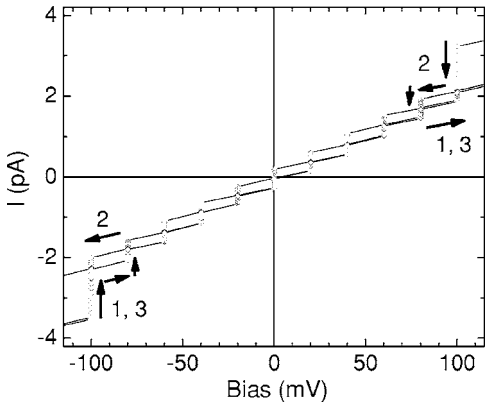

FIG. 7. Settling test measurement.

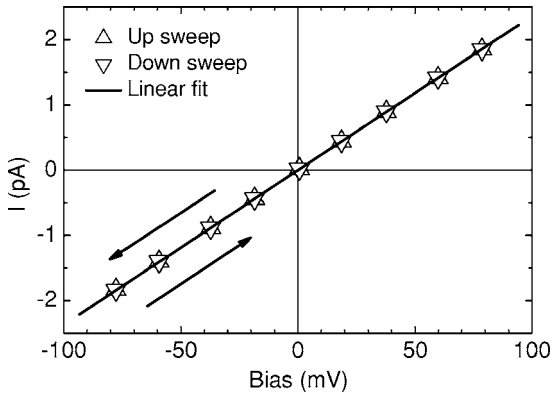

FIG. 8. Bias corrected $I(V_B)_{\text{settle}}$ data and the (practically identical) linear fits of the up and down sweeps.

triax connection to the electrometer's chassis ground and the electrometer LO's were also connected to the enclosure. Teflon insulation inside the enclosures had to be cleaned and dried frequently for precision measurements of zero-bias offsets to eliminate leakage paths due to moisture deposition from ambient air. The voltage source of one electrometer was used to bias the CdZnTe test devices. The nominal (set point) bias voltages had to be corrected for the source-range dependent actual output voltages of the specific device, especially when operated below 100 mV. Guard ring and center electrode were, in most cases, kept at ground potential during the measurement. Note that there can be a small offset voltage present at the amplifier inputs of the Keithley-6517A feedback ammeters, so that the guard and center electrodes are not exactly at the same potential anymore (configuration shown in Fig. 4). Those offset voltages cannot be exactly compensated with the electrometer calibration routine and may remain in the $\pm(10-50)$ μV range. Consequently, a center-to-guard leakage path can slightly influence the electrometer readings, especially, on devices with a relatively small gap between guard and center electrodes. For example, with a center-to-guard resistance of 1 GΩ, a 50 μV amplifier offset voltage produces a 50 fA zero-bias offset reading. However, generating an adequately passivated, low-leakage surface between the center and guard electrodes of the CdZnTe test device can eliminate this problem.

Furthermore, the measurement has to take care of the various charging effects due to cable capacitances and crystal defects. The latter can lead to quite unpredictable time dependences of the current settling characteristics $I(t)$. We implemented a dynamic evaluation routine of the sampled $I(t)$ data to always ensure adequate current settling while not spending unnecessary time if the settling was fast. An independent verification of proper settling was obtained by conducting the standard measurements as "voltage up-and-down sweeps," i.e., the data acquisition program was running through the same bias steps a second time but in reverse order and evaluated the relative slope deviation of the linear up- and- down-fit results as an additional measurement goodness parameter. Figure 7 shows an example of such a settling test were the bias was swept in an up(1)-down(2)-up(3) sequence in small steps between -120 and $+120$ mV. The $I(t)$ data were continuously recorded and the whole data set was then plotted in an $I(V_B)$ diagram, i.e., the $I(t)$ settling at each bias voltage is now visible as a vertical step that approached the same final $I(V_B)_{\text{settle}}$ value, independently of the sweep direction. Figure 8 shows bias corrected $I(V_B)_{\text{settle}}$ data and the (practically identical) linear fits of the up and down sweeps.

For our bulk resistivity measurements, an even smaller bias range (± 30 mV) was normally used.

VI. BULK RESISTIVITY

With the configuration of Fig. 4, the bulk resistivity is given by $\rho_{\text{bulk}}=R_C(A_{\text{center}}/d)$, where R_C is the inverse slope of the linear fit of the center electrode's $I(V_B)_{\text{settle}}$ data d is the detector thickness, and A_{center} is the average effective cross section of the current path under the center electrode. In principle, the current path can be confined to roughly the geometrical size of the center electrode by keeping the gap between the center and guard electrodes small and operating both at the same potential. This approach, however, becomes an accuracy trade-off when the resistance between these two electrodes is getting too small. A spreading estimate for the unconfined case with a 5×5 mm^2 center electrode and an infinite-size bottom contact would yield about 1 mm spreading beyond the geometrical size of the center electrode at a detector depth of 2 mm.[14] With an actual 10×10 mm^2 bottom electrode, however, the current path obviously does not spread more than 0.5 mm. This has been experimentally verified for a 1 mm gap pattern by biasing the center electrode and reading the current from the bottom. Since the guard and bottom electrodes are at the same potential now, there is no field line confinement under the gap anymore. Yet, the measured center resistance was exactly the same as for the conventional configuration, which puts an upper limit of $\pm 9\%$ on the possible spreading related systematic error in ρ_{bulk}. From this point of view, a larger center electrode and a thinner test part will reduce the relative error.

To prove experimentally that there is no significant contribution of the contact barrier on the measured bulk resistance in the low-bias regime we conducted a series of reprocessing (various surface processing and contact metal) and thinning experiments on the same CdZnTe crystals. In the latter test, the same crystals were thinned in several steps from 10 mm thickness gradually down to 2 mm and the

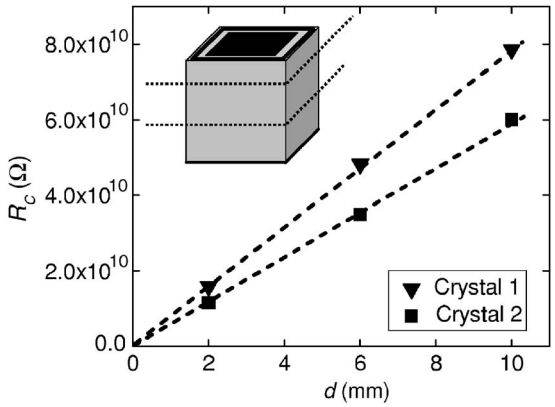

FIG. 9. Measured low-bias bulk resistance in dependence on crystal sample thickness. (The effective center electrode area is ~0.82 cm^2.)

same guarded electrode pattern was reapplied every time. The resulting $R_C(d)$ plot was linear and could be extrapolated without any zero offset (Fig. 9). The effective center electrode area was ~0.82 cm^2 in this example and the gap to the guard electrode was only 100 μm to keep the spreading error small.

VII. SURFACE RESISTIVITY

In the equivalent circuit shown in Fig. 4(b), the side surface resistance R_S can be obtained by separating the bulk contribution R_{BG} from the total guard resistance (R_{guard}) according to

$$\frac{1}{R_S} = \frac{1}{R_{\mathrm{guard}}} - \frac{A_{\mathrm{guard}}}{\rho_{\mathrm{bulk}} d}, \tag{6}$$

with A_{guard} being the effective cross section of the bulk current path under the guard electrode. The corresponding normalized quantity is

$$\rho_{\mathrm{surface}} = R_S \hat{u}/\hat{d}, \tag{7}$$

where $\hat{u}$ and $\hat{d}$ are the effective circumference and the height of the side surfaces also accounting for nonmetalized gaps between the guard electrodes and the actual edge of the detector . ρ_{surface} is the side surface resistivity, which is equivalent to the resistance between opposite edges of a square of that surface, i.e., it describes the effect of the surface rather than a specific surface layer property because neither the thickness of the "film" nor its profile are known. It is, however, a quantity that is independent of the device and electrode pattern geometry and can be used to compare surface properties of detectors with different geometries and fabricated with different surface processing methods.

VIII. TEMPERATURE NORMALIZATION

In general, semi-insulating semiconductors show a strong temperature dependence of the free carrier concentration in any temperature range, which can lead to significant misjudgments when comparing resistivity data obtained under only slightly different laboratory temperature conditions. Rather than stabilizing the measurement temperature (T_{meas}), we implemented a normalization procedure for the ρ data to

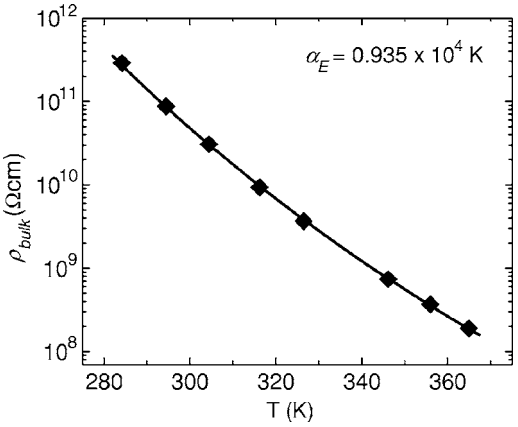

FIG. 10. Temperature dependent bulk resistivity measurement on a SI-CdZnTe test device in the range between 284 and 365 K. The line is a fit according to Eq. (8) yielding $\alpha_E = 0.935 \times 10^4$ K.

a reference temperature (T_{ref}) that was closest to the usual average laboratory temperature (296 K). For the ideal intrinsic case [Eq. (1)], the temperature dependence of the resistivity is mainly governed by the $\exp(E_g/2k_BT)$ term, where the temperature dependence of the band gap $E_g(T)$ is only of minor influence and consequently, a convenient normalization from $\rho(T_{\mathrm{meas}})$ to $\rho(T_{\mathrm{ref}})$ is already provided by

$$\rho(T_{\mathrm{ref}}) = \rho(T_{\mathrm{meas}}) \exp\left[\alpha_E^* \left(\frac{1}{T_{\mathrm{ref}}} - \frac{1}{T_{\mathrm{meas}}} \right) \right]. \tag{8}$$

Comparison of Eq. (8) with Eqs. (1)–(3) yields an intrinsic slope factor $\alpha_E^{\mathrm{intr}} \sim 1.02 \times 10^4$ K, which is naturally close to $E_g/2k_B$. For real SI-CdZnTe, the temperature dependence of the resistivity around RT is governed by the ionization energies of the compensating deep defects but can still be approximated by a linear $\ln \rho(1/T)$ slope, which will be only slightly different from the intrinsic case, i.e., $\alpha_E \sim \alpha_E^{\mathrm{intr}}$. This is because those Fermi level pinning deep have to be close to the middle of the band gap (SI material) and for the small temperature variations that are of practical interest, a reasonable accuracy is already achieved by using the normalization equation (8) with α_E^{intr}. This is illustrated in Figs. 10 and 11. Figure 10 shows the result of an actual temperature dependent bulk resistivity measurement on a SI-CZT test device

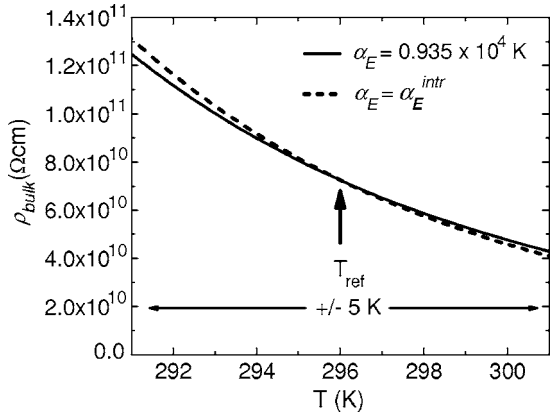

FIG. 11. Comparison of the temperature dependence of the bulk resistivity of the test device from Fig. 10 with the intrinsic slope ($\alpha_E^{\mathrm{intr}} \sim 1.02 \times 10^4$ K) in a ±5 K temperature window around $T_{\mathrm{ref}} = 296$ K.

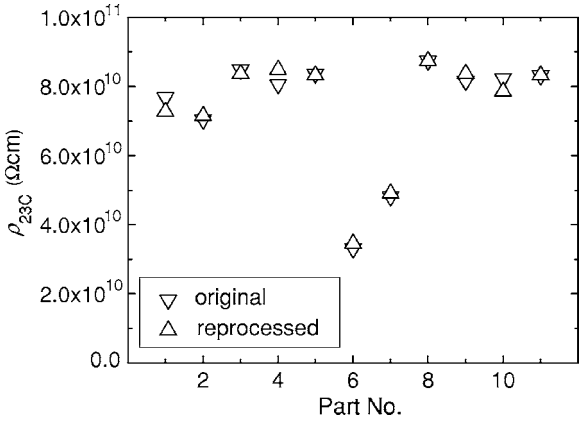

FIG. 12. Measured bulk resistivity data of a set of CdZnTe samples from different ingots before and after reprocessing.

with guard electrode in the range between 284 and 365 K. The line is a fit according to Eq. (8) yielding $\alpha_E = 0.935 \times 10^4$ K for this particular crystal (only ~8% deviation from α_E^{intr}). Within a ±5 K temperature window around T_{ref}, however, the effect of this deviation on the bulk resistivity becomes practically negligible as shown in Fig. 11.

IX. EXAMPLES

A. Reprocessing

Figure 12 shows the result of an experiment in which the bulk resistivities of a number of crystals from different CdZnTe ingots/ingot sections were measured before and after reprocessing, i.e., the electrodes were removed and the devices were refabricated with the same electrode geometry but using a different surface preparation and metal deposition process. The obtained normalized bulk resistivity data ρ_{23C} ($T_{\text{ref}} = 296$ K) were practically identical, independent of the different fabrication methods.

B. Surface passivation

Figure 13 shows an application of the surface resistivity concept: Bulk and surface resistivities of a number of devices from the same CdZnTe crystal slice were measured before and after a surface passivation process has been applied. The effect of the passivation can now be quantified in terms of surface resistivity, which increased by about one order of magnitude in this example. The bulk resistivity results did not change as a result of this treatment.

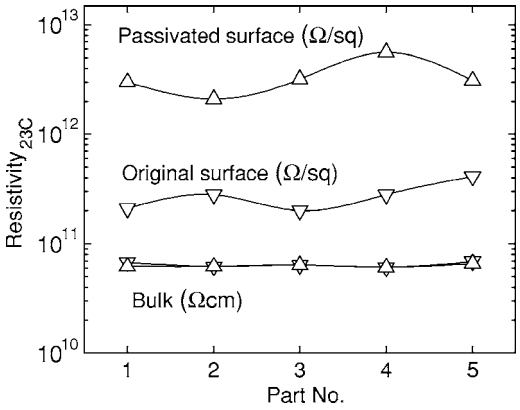

FIG. 13. Passivation effect on the surface resistivity of a set of CdZnTe detectors. The bulk resistivity data did not change.

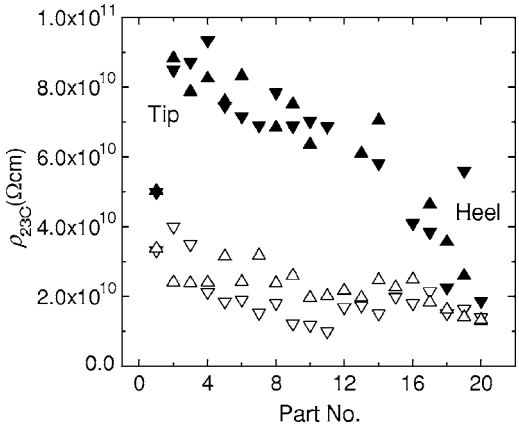

FIG. 14. Tip-to-heel 23 °C-resistivity profile of a $Cd_{0.9}Zn_{0.1}Te$ ingot measured on devices in the dual *I-V* guard electrode configuration (filled triangles) and erroneous data from measurements on devices with a simple parallel plate electrode configuration (open triangles). Two neighboring rows of $5 \times 5 \times 2$ mm^3 axial parts have been examined for each of the configurations (upside and downside tipped triangles).

To illustrate the numbers, a $10 \times 10 \times 2$ mm^3 parallel plate device (i.e., using full-area contacts without the guard electrode) with a bulk resistivity of 5×10^{10} Ω cm would require a surface resistivity of at least 2×10^{11} Ω/sq to ensure that most of the low-bias current is flowing through the bulk of the crystal. The higher the bulk resistivity the better passivation is required to satisfy this condition. For lower surface resistivity, the side surface leakage dominates the measured current and the erroneous "bulk" resistivity value extracted in a configuration without the guard electrode will be significantly smaller than the true value.

C. Axial resistivity profile

Figure 14 shows an application of precision measurements to determine the distribution of the bulk resistivity along the growth direction of a CdZnTe ingot. Two axial rows of $5 \times 5 \times 2$ mm^2 test crystals have been cut out from tip to heel of a CdZnTe ingot grown by the high-pressure electrodynamic gradient technique. The samples were fabricated into test devices in the guard electrode configuration, and a temperature normalized axial bulk resistivity profile was measured. Such an accurate bulk resistivity profile is a helpful tool to develop and evaluate electrical compensation models of CdZnTe ingots.

For comparison we also show the resistivity data, which were obtained from measurements on parallel plate test devices without the guard electrode from two other (neighboring) axial rows of crystal samples from the same ingot. In this case, the side surface leakage contributed to the resistance measurement and led to a serious error in the "bulk resistivity" results. This error tends to be less significant the lower the bulk resistivity and the better the surface passivation are. This can be seen in Fig. 14. As the bulk resistivity drops (approaching the heel of the ingot) the values obtained

on the parallel plate devices deviate less from the accurate values obtained on devices with guard electrodes.

X. SUMMARY

Part of the confusion with published resistivity data for SI-CdZnTe detector material can be attributed to the often erroneous or misinterpreted measurements mostly due to the neglected Schottky barrier effect at the electrodes, surface leakage contributions, and temperature dependences. In this paper we discussed some fundamental requirements and considerations to accurately determine the true bulk resistivity at a certain temperature and to adequately and reliably separate and quantify surface contributions to the overall leakage current of semi-insulating CdZnTe detector crystals. Reference temperature normalized low-bias dual *I-V* measurements on devices with guard electrodes have been evaluated and shown to be a powerful and accurate technique to accomplish this goal.

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