Test Results of a CdZnTe Pixel Detector Read Out by RENA-2 IC

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***Abstract*-- A new mixed signal integrated circuit (IC) for front-end readout electronics of position sensitive solid state detectors has been developed. It is called RENA-2 and can be used for readout of position sensitive solid state detectors such as CdTe, CdZnTe, Ge, GaAs, HgI_2, PbI_2, Se and Si strip, pad and pixel detectors, with large numbers of channels. It is designed to have very low noise and, therefore, high energy resolution. It has numerous possible applications in astrophysics, medical and industrial imaging, security such as baggage inspection and nuclear physics. The RENA-2 chip is a monolithic integrated circuit and has 36 channels with low noise, high input impedance charge sensitive amplifiers. The RENA-2 chip can be optimized for individual applications.**

I. Introduction

THE RENA-2 chip (Fig. 1) is related to the earlier RENA IC (**R**eadout **E**lectronics for **N**uclear **A**pplications IC) [1] in functionality only. It embodies a completely new design with extensive features to render it versatile to meet the requirements of many different applications.

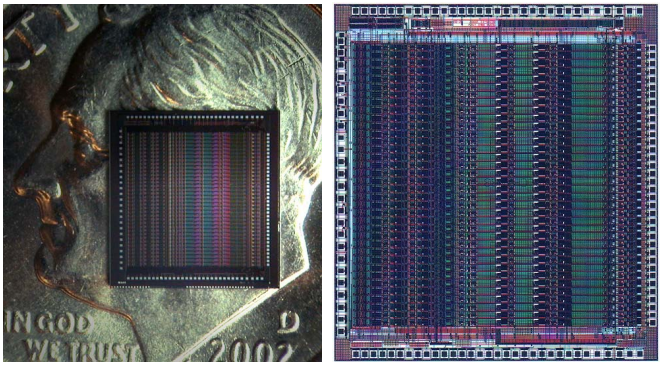

Fig. 1. On the left is a photograph of the RENA-2 IC placed on top of a dime to show its size. On the right is the actual silicon layout of the RENA-2 chip, implemented in the 0.5 micron AMI process.

RENA-2 IC features include the chip's low-noise performance, self-trigger capability and versatility in providing different peaking times, several readout modes and the daisy-chain option [2]. Specifically, the peaking times were made adjustable from about 0.4 to 40 microseconds, which makes the chip suitable for a wide range of detectors, from CdZnTe to HgI_2. The input amplifier was designed to tolerate leakage current so that detectors can be DC–coupled, thus eliminating the need to use capacitive AC coupling. The comparator thresholds are individually adjustable through an eight-bit DAC on each channel. This allows accurate and uniform threshold setting throughout the detector. Other innovative features include user-selectable dynamic range, fast trigger output for coincident event detection and the ability to provide channel-by-channel time difference information. The new chip also incorporates a pole zero cancellation circuit to handle large rates without significant pileup. Two important new features for space deployment are the ability to adjust power consumption by limiting the current flow to the input transistor and the radiation hardness inherent to the 0.5 micron CMOS process and augmented by special layout techniques. Four extra channels were moreover added to allow connecting the common electrode of a pixel detector to the same IC as its pixel electrodes. Further, the chip interface was streamlined and unnecessary connections were eliminated to enhance functionality.

II. RENA-2 IC Description

RENA-2 is a 36-channel mixed signal ASIC chip with low-noise self-resetting charge sensitive preamplifiers at the input of each channel (Fig. 2). The extra channels are built in to allow connection to the common electrodes of solid state pixel detectors. Each channel has two individually selectable dynamic ranges for wide energy range applications (≈ 9 fC and ≈54 fC). The chip is designed for ultra-low noise (simulations show 45 to 120 e rms input referred noise for each range @ 0 pF input capacitance.) The inputs are single-ended to improve noise performance. Channel-by-channel selection of negative or positive input polarity allows signal detection from both the anode and cathode on the same detector. A sparse readout mode is available for reading out only the channel, which contain data. Another option is an on-chip generalized neighbor readout mode, which can be applied for both strip and 2-D pixel array detectors. RENA-2 features low power operation ≤ 5.8 mW/Ch for space based astrophysics applications. Power consumption is adjustable. Also full or

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partial power down is available on a channel-by-channel basis. The chip is optimized for two input capacitances (2 pF & 9 pF selectable channel-by-channel).

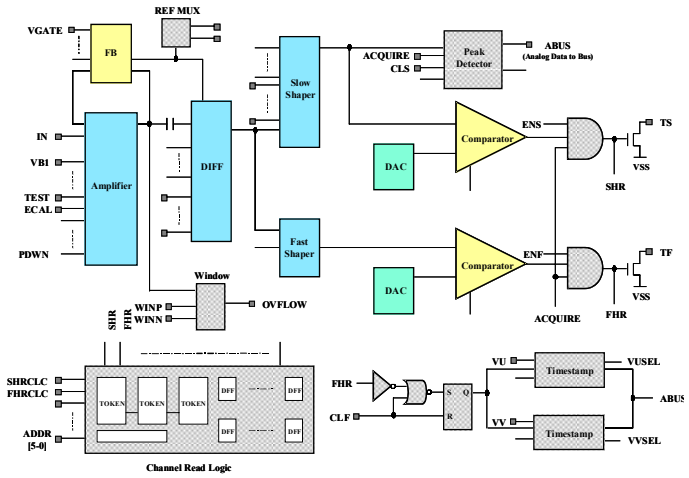

Fig. 2. RENA-2 IC single channel block diagram showing all the analog circuitry and some of the control system.

One of the most important features of RENA-2 is its self-resetting charge-sensitive input preamplifier (Fig. 2). The self-resetting function restores the increase in pedestal produced by the detector leakage current and eliminates the need for AC coupled connection between the detector channel and the input amplifier. Therefore, RENA-2 has been designed with built-in tolerance for detector leakage current (< ± 5 nA) and it can be DC coupled to most position sensitive solid state detectors.

RENA-2 also has selectable peaking times from 0.4 to 40 µs in 32 steps. This extensive range of peaking times allows RENA-2 to be used for many different kinds of solid state detectors, from fast silicon pixel and strip detectors to much slower Ge and HgI_2 detectors. It also has a high resolution and accurate peak and hold circuit for carrying out high energy resolution spectroscopy with ease.

The RENA-2 chip is designed to have a self-trigger output capability using a comparator (Fig. 3). The self-trigger output is especially important for nuclear and radiography applications where the incident photon is random and its arrival time is not known.

Some applications require accurate (low jitter) fast timing signals for coincident imaging such as positron emission tomography (PET) and double Compton scatter detectors. RENA-2 is designed to accommodate such applications by incorporating a fast low jitter shaping and comparator circuit on each channel (Fig. 3). This circuit produces a fast timing trigger output, which is separate from the slow event trigger output. The slow trigger output provides accurate pulse-height discrimination for event triggers and must be used for recording an event, and the fast trigger should be used in conjunction with the event trigger for coincidence determination. Another interesting functionality built into the RENA-2 chip is the time stamp circuit at each channel (Figs. 2 & 3). This circuit utilizes user-supplied time-variable signals to produce data on channel-to-channel pulse arrival time difference. This feature can be useful if information on the arrival time differences for multiple simultaneous events is required.

RENA-2 also has a second slow comparator (Fig. 3) that triggers whenever the input signal exceeds the dynamic range of the amplifiers. In RENA-2 provisions were made to enable fine tunable compensation for channel-to-channel and chip-to-chip fabrication variations. For example, an adjustment of comparator thresholds for each channel is achieved by using a DAC at each comparator.

The RENA-2 chip may be used in fast photon counting applications. To achieve smooth fast photon counting at short peaking times, a pole zero cancellation circuit, which reduces pulse pileup for high input signal rates was incorporated into the IC. Up to eight RENA-2 chips can be wired together to be read out as a single chip with 288 channels. This feature will be useful for large channel low rate applications. The chip has a low noise differential analog output to preserve its low noise high energy resolution capability.

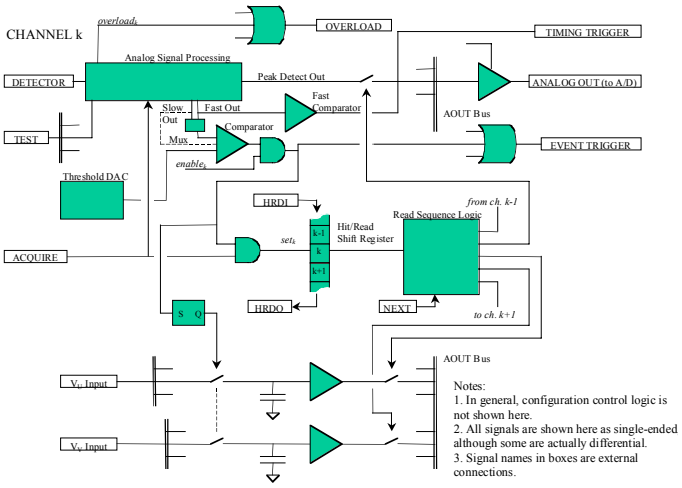

Fig. 3. Schematic diagram of the RENA-2 ASIC. Only one channel (Channel k) is shown; connections to adjacent channels are indicated where applicable; the slow and fast signals are shown multiplexed.

III. RENA-2 Specifications and Applications

The key RENA-2 key design features and general specifications are listed in Table I. Table I also shows the many new features RENA-2 chip has to make it a versatile and flexible integrated circuit to address the needs of many different applications.

RENA-2 can therefore be used for many different applications in medical, industrial, NDI and security fields. A long list of target detector applications is available. Most of the applications are for imaging x-rays and gamma rays. However, the chip can be used with any detector or system that produces charge pulses in the time frame of picoseconds to microseconds.

RENA-2 is also developed with many interesting and different features so that it can be tested and investigated for

different applications. Once the investigation is complete and the chip is found that it will work, then it can be optimized for each application and unneeded circuits can be also taken out.

Table I. Key design criteria and features of the RENA-2 IC.

Signal range:	Two full-scale ranges; 50 and 250 ke, selectable for each channel
Input polarity:	- or + (Selectable channel-by-channel)
Number of channels:	36 (extra channels to allow connection of common electrode)
Noise:	Minimize noise (112 e rms in lower signal range; 280 e rms in higher with a detector connected)
Noise optimization:	2 pF and 9 pF detector capacitance
DC leakage current:	Minimized & tolerant up to 25 nA leakage current
Power consumption:	< 5.8 mW per channel
Fast timing output:	Jitter minimized by use of fast shaping
Channel-channel time difference:	Implement
Power consumption:	Adjustable
Trigger comparator thresholds:	Individually adjustable by internal 8 Bit DACs for each channel
Peaking times:	0.36 to 38 microseconds in 16 steps
Fast count rates:	Using pole zero cancellation
Detector structure:	Heterogeneous or homogeneous
Key gamma signals:	14 keV, 60 keV, 141 keV, 511 keV, 662 keV, up to 1.33 MeV
System components:	Pipeline A/D converter, FPGA state machine controller, data FIFO
Interface:	Minimum pin count; support component count
Readout mode:	Maximum flexibility through hit register
Deadtime per event:	Minimized
Radiation tolerance:	Minimize effects by use of standard rad hard layout techniques to about 0.1 to 1 MRad

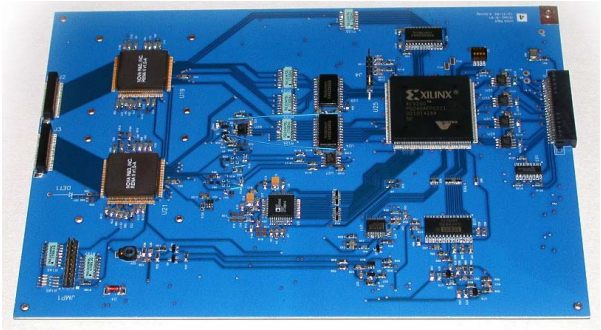

Fig. 4. RENA-2 test PC board, which can accommodate up to two RENA-2 chips shown on the left with two standard connectors to mount detector(s). The RENA-2 chip can also be mechanically clamped to the board for initial acceptance tests. The large XILINX chip on the right is the FPGA that controls the whole test board and the RENA-2 IC.

IV. RENA-2 IC Test System

A RENA-2 test system has been developed to test the new IC. Fig. 4 displays a photograph of the RENA-2 test board. As seen in Fig. 4 and shown explicitly in Fig. 5, the standard mounting solution chosen for the RENA-2 chip is to assemble it inside a readily available CQFP package. This choice reduces cost and facilitates chip testing (the packaged chip can be mechanically clamped to the test board to establish electrical contact), thus aiding application development and commercialization.

V. RENA-2 IC Diagnostic Features

Every channel of the RENA-2 has a test pulse input (707 mV step injects full scale signal ≈ 53 fC). The test pulses can be turned on and off individually for each channel. This capability allows for testing the chip without a detector. RENA-2 also has several diagnostic modes. For example, the follower mode bypasses the peak hold circuit and connects the shaper output directly to the output of the channel. The force-enable mode provides the capability of continuous monitoring of the peak detector or shaper output of any externally selected channel. There are also probe pads provided on the chip layout to test critical sections of the IC using probes.

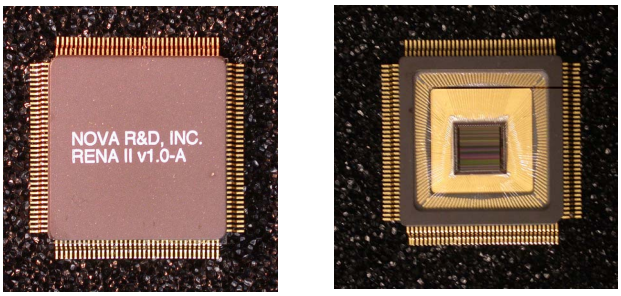

Fig. 5. Photograph on the left shows the RENA-2 IC mounted inside a CQFP package. Photograph on the right shows the wire bonded RENA-2 IC inside the CQFP package.

VI. RENA-2 IC Preliminary Test Results

The RENA-2 IC noise was simulated during the design phase. The results show that at 0 pF detector input capacitance the input referred noise can be as low as 45 and 60 e rms for low and high dynamic range modes, respectively. The power dissipation for each channel was also simulated. The results show ≈ 5.8 mW per channel maximum power dissipation.

Tests were performed on the fabricated RENA-2 prototype chips (Fig. 5) using the above-described test board (Fig. 4).

Fig. 6 shows noise measurements for different detector input capacitances plotted for the two externally selectable detector capacitance ranges, 2 and 9 pF. The preliminary measurements show that 0 pF detector capacitance results in ≈ 140 and

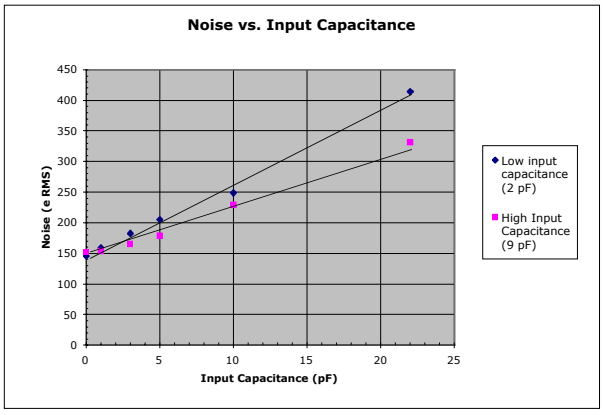

Fig. 6. Noise is measured and plotted for different detector input capacitance values for the two externally selectable detector capacitance ranges, 2 and 9 pF.

150 e rms noise at room temperature, respectively, for these two detector capacitance ranges.

Fig. 7 shows a RENA-2 linearity measurement. The output pulse heights were measured with an oscilloscope set for continuous average with a weight of 1:15. The input pulse was put through a 1pF capacitor mounted directly on the detector input to the IC channel. The RENA-2 chip was configured for maximum channel gain. The red vertical line near the center shows the design limit for the lower energy (higher gain) dynamic range, 200 keV.

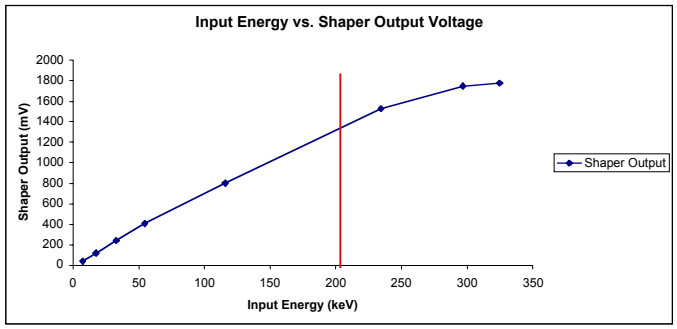

Fig. 7. RENA-2 IC linearity measurement.

X-ray spectra were also acquired simultaneously on multiple channels of the prototype RENA-2 IC. Fig. 8 shows a Co-57 single pixel spectrum measured at room temperature using a 1.75 mm thick CdZnTe pixel array with 2 x 16 pixels at 1 x1 mm^2 pixel pitch, fabricated by eV Products. The energy resolution is 3.7 keV FWHM at 122 keV. Fig. 9 shows x-ray spectra from an Am-241 source obtained using a 3 mm thick CdZnTe 2 x 16 pixel array also with 1 x 1 mm^2 pixel pitch. The spectra were acquired simultaneously at 3 °C ambient temperature with two channels connected to two pixels of the array. The energy resolution is 3 keV FWHM @ 60 keV. Only raw data were used to produce the spectra without any processing.

VII. Conclusion

Initial results of tests on the RENA-2 chip have been quite encouraging. Full characterization of this chip is currently underway with an eye on performance parameters and functionalities that can find immediate use in instrument prototyping; aspects of the design requiring revision for the next version are also being determined. "Daughter" chip designs based on the versatile, multi-feature RENA-2 can be envisioned as custom readout solutions optimized for specific x-ray and gamma-ray spectroscopy applications.

VIII. Acknowledgments

We gratefully acknowledge the members of the RENA-2 Consortium for partially supporting the development and testing of the first version of the RENA-2 IC. We also thank D. Ward and G. Visser for helpful discussions on chip testing.

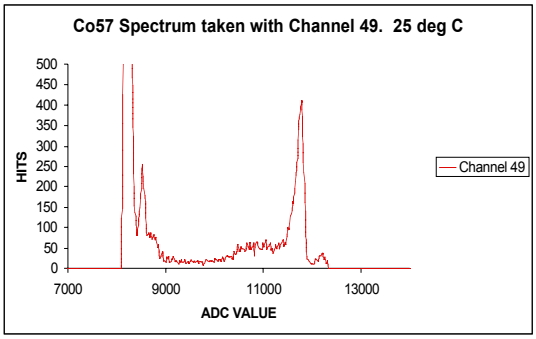

Fig. 8. RENA-2 IC Co-57 single pixel spectrum measured at room temperature using a 1.75 mm thick CdZnTe pixel array with 2 x 16 pixels at 1 x 1 mm^2 pixel pitch, fabricated by eV Products.

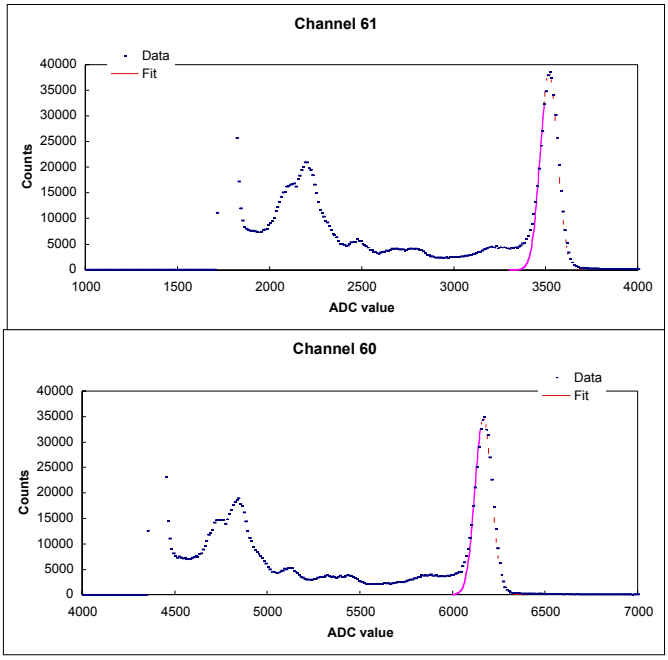

Fig. 9. RENA-2 Am-241 two pixel (channels 60 & 61) preliminary spectra measured at 3 °C ambient temperature using a 3 mm thick CdZnTe pixel array of 2 x 16 pixels with 1 x 1 mm^2 pixel pitch. Energy resolution is 3 keV FWHM @ 60 keV for both spectra.

IX. References

[1] Kravis, S.D., Maeding, D.G., Tümer, T.O., Visser, G., Yin, S., "Test Results of the Readout Electronics for Nuclear Applications (RENA) Chip Developed for Position-Sensitive Solid State Detectors," SPIE Symposium Proceedings 3445, 374 (1998). Available at http://www.novarad.com/pages/documents/RENA_test_results_SPIE_1998.PDF.

[2] a) Tümer, T.O., V.B. Cajipe, M. Clajus, H. Flores, C.A. Shirley, G. Visser, and D. Ward, Preliminary Test Results of RENA-2 ASIC Developed for Position-Sensitive X-ray and Gamma-Ray Detectors, contribution to the 2002 IEEE Nuclear Science Symposium, Norfolk, VA, Nov. 2002; b) Tümer, T.O., V. Cajipe, A.C. Shirley, M. Clajus, S. Hayakawa, G. Visser, J. Matteson and D. Ward, Preliminary test results of a low-noise integrated circuit (IC) developed for position sensitive solid state detectors, contribution to the International Symposium on Optical Science and Technology (SPIE's 48th Annual Meeting and Exhibition), San Diego, CA, August 2003.