Integrated Readout Electronics: Enabling Advanced Applications of Position-Sensitive Solid-State Radiation Detectors

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Abstract-- **As applications of advanced solid-state radiation detector arrays proliferate across disciplines ranging from x-ray astronomy and medical imaging to security and industrial inspection, the relative scarcity of low-noise, multi-channel integrated circuits (ICs) needed to read out these arrays has become increasingly apparent. In fact, readout ICs are now regarded to be an integral part of position-sensitive semiconductor detectors for x-ray and gamma-ray imaging. Because the requirements of various detector applications tend to be diverse, a custom IC is typically designed for a specific detector array. This often lengthens the time and raises the cost of system development. To help close the readout technology gap and facilitate advances in this field, NOVA has been formulating strategies for instrumenting different detectors of a given application category with the same "generic" IC which embodies common functions as well as selectable features. A brief overview of possible approaches to such generic ICs will be given. Within this context, accomplishments and ongoing efforts at NOVA in developing front-end ICs for various detector architectures and signal-processing scenarios will be described. We will especially consider the case of ICs used in conjunction with position-sensitive CZT detectors, implemented in traditional soldered lead or flip-chip connection geometries, to perform spectroscopic, energy-binning or current-mode type measurements.**

I. INTRODUCTION

APPLICATIONS of position-sensitive solid-state radiation detectors have grown rapidly in recent years as a consequence of parallel advances in detector materials science and low-noise microelectronics design [1], [2]. The sensor and signal processing components of a detector module have increasingly assumed monolithic forms, i.e., pixel or strip arrays and multi-channel integrated circuits (ICs), respectively. Whereas the concept for a given detector application often revolves around the characteristics and capabilities of a sensor array, actualizing an instrument design assumes that the matching readout electronics are already available or will be developed as part of the program. As such, it has become generally recognized that readout ICs and their associated support electronics are an essential and integral part of a detector unit. Ideally, a readout IC would be designed to meet the specific performance requirements of a given application. Custom chip development can however be a time-consuming, high-risk and financially onerous undertaking which most R&D projects cannot afford. Broadening the applicability and accessibility of readout ICs that do get development funding would therefore benefit manifold efforts to prototype emerging detector designs. To this end, one could adopt a "generic IC" approach, premised on the fortune of direct sponsorship that is virtually independent of instrument development. This would proceed by: identifying commonalities within an application category; defining corresponding generic IC classes; and, developing an IC for the requirements of each class. More realistically, since most new chip designs are carried out within an application development program, one could simply expand the features of the application-specific IC (ASIC) in question. This approach would provide ranges and options for key specifications and accommodate additional functions as far as technically and logistically reasonable.

We have taken both approaches in developing readout ICs. Fig. 1 outlines our IC development roadmap divided according to detector application class. Under the spectroscopy category is the RENA™ [3] family of chips. We have developed an all-new "RENA-2" version of this linear multi-channel chip as a generic IC; a chip named "DANA" with a similar channel design repeated over a two-dimensional (2D) array has also been fabricated. Energy-binning applications form another important class for which we developed the FESA™ IC [4] and, more recently, the linear XENA™ [5] and 2D HILDA™ IC. For imaging with high spatial resolution, the third application category, we have the MARY™ [6], a TDI CCD readout channel array chip which has evolved into MARY-2 and MARY-3 versions. In the following sections we give brief descriptions of the afore-mentioned ICs [7].

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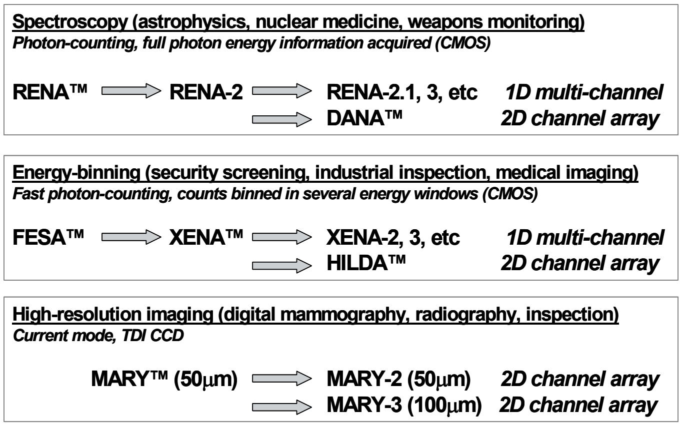

Fig. 1. NOVA's IC development roadmap.

II. SPECTROSCOPY

A. RENA-2

The RENA-2 is a 36-channel low-noise, self-resetting, charge sensitive amplifier/shaper IC with trigger output, wide energy range and sparse readout for use with position-sensitive, spectroscopy-grade detectors. Its design was based on our experience with the older RENA (**R**eadout **E**lectronics for **N**uclear **A**pplications) chip and the detector application requirements of RENA users who formed a consortium to support this generic IC development. The breadth of specifications covered in the RENA-2 design can be gleaned from the detector characteristics gathered in Table I. Fig. 2 shows an example spectrum acquired with the RENA-2 as well as a picture of a bare RENA-2 die. The key features of the chip are gathered in Table II.

TABLE I
DETECTOR CHARACTERISTICS CONSIDERED IN RENA-2 IC DESIGN.

Application	Full-scale signal	Electronics noise, rms	Capacitance	Leakage	Charge collection
CZT strip detector for astrophysics (anodes)	1.33 MeV	1 keV	0.5 pF	1 nA	50 ns
CZT strip detector for astrophysics (cathodes)	1.33 MeV	4 keV	10 pF	20 nA	50 ns, 550 ns
CZT pad detector for gamma camera	141 keV	500 eV	4 pF	2 nA	50 ns, 550 ns
CZT small pixel detector for astrophysics	1.33 MeV	1 keV	0.5 pF	250 pA	50 ns
Ge detector for astrophysics	1 MeV	840 eV	10 pF	50 pA	20 ns
Si detector for astrophysics	1.2 MeV	1 keV	10 pF	1 nA	20 ns
HgI_2 detector	1.5 MeV	1 keV sigma	5 pF	50-250 pA	40μs peaking
Silicon detector for electrons	300 keV	3 - 6 keV	20 - 40 pF	6 - 20 nA	≈ 1 ns
Silicon detector for light ions	1.5 MeV	3 - 6 keV	10 - 20 pF	6 - 20 nA	700 ps
Large active volume CZT detector	1.33 MeV	1.25 keV	3 pF	5 nA	50 ns
CZT detector for astrophysics	1 MeV	1 keV	8 pF	5 nA	50 ns, 550 ns

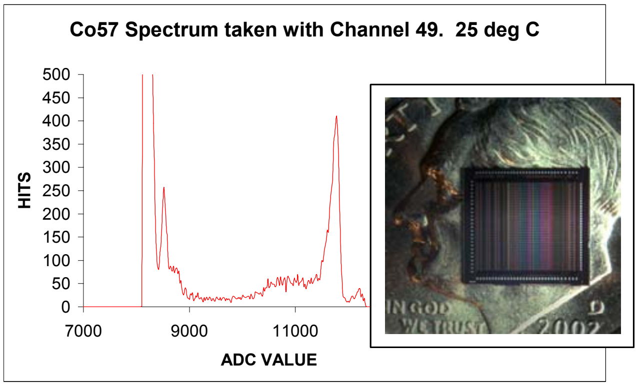

Fig. 2. Example of single-pixel ^{57}Co spectrum obtained using the RENA-2 IC with a 2 x 16 CZT pixel array. Inset: Photograph of a RENA-2 die on a dime.

TABLE II
KEY FEATURES OF THE RENA-2 IC.

Signal range:	Two full-scale ranges; 50 and 250 ke, selectable for each channel
Input polarity:	Selectable channel-by-channel
Number of channels:	36 (extra channels to allow connection of common electrode)
Noise:	Minimize noise (112 e rms in lower signal range; 280 e rms in higher)
Noise optimization:	2 pF and 9 pF detector capacitance
DC leakage current:	Minimize effects and to be tolerant
Power consumption:	Minimize power
Fast timing output:	Minimize jitter as far as possible
Channel-channel time difference:	Implement
Power consumption:	Adjustable
Trigger comparator thresholds:	Individually adjustable by internal 8 Bit DACs for each channel
Peaking times:	0.36 to 38 microseconds in 16 steps
Fast count rates:	Using pole zero cancellation
Detector structure:	Heterogeneous or homogeneous
Key gamma signals:	14 keV, 60 keV, 141 keV, 511 keV, 662 keV, up to 1.33 MeV
System components:	Pipeline A/D converter, FPGA state machine controller, data FIFO
Interface:	Minimum pin count; support component count
Readout mode:	Maximum flexibility through hit register
Deadtime per event:	Minimize as far as reasonable
Radiation tolerance:	Minimize effects as much as possible with standard process to about 0.1 to 1 MRad

B. DANA

The DANA IC (**D**etector **A**rray for **N**uclear **A**pplications **I**ntegrated **C**ircuit) is a 16 x 16, 500mm pitch array of channels with a charge sensitive amplifier/shaper, trigger output and sparse readout intended for use in flip-chip connection with a spectroscopy-grade 2D detector pixel array. It is in effect a 2D incarnation of the RENA-2; it also takes heritage from an earlier 2D channel array chip developed for x-ray astrophysics [8] and investigated for use in molecular imaging. The advantages of such a readout channel array include lower input capacitance and noise, finer pixel pitch, more compact sensor-readout assembly and ease of tiling array units into a large-area 2D array. On the other hand, its format entails the challenge of fitting complex circuitry within the unit cell area, developing the matching detector pixel array, and finding a solution for reliable and cost-effective IC-detector bonding.

Fig. 3 displays images of the DANA IC layout and fabricated die while Fig. 4 shows the block diagram for a single signal chain of the chip. The key features of DANA are summarized in Table III.

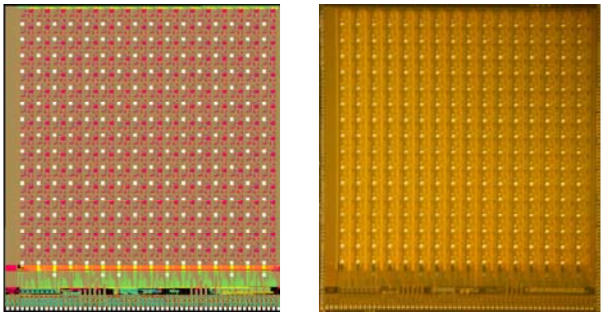

Fig. 3. Layout (left) and photograph (right) of the DANA IC.

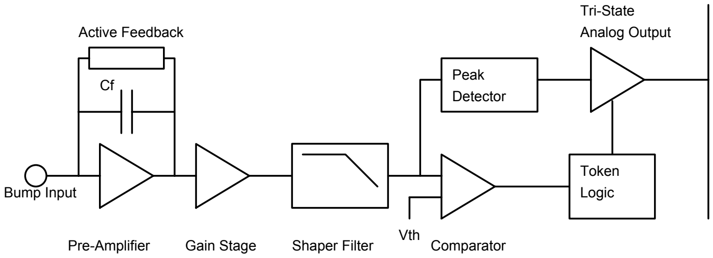

Fig. 4. Block diagram for a single signal chain of the DANA IC.

TABLE III
KEY FEATURES OF THE DANA IC

Number of channels:	16x16 matrix, 500μm pitch
Frond end:	Self-resetting charge sensitive amplifiers
Input energy range:	≈ 1-150 keV
Input polarity:	Positive and negative
Count rate capability:	> 400 x10^3 counts/sec, all channels in parallel
Gain and offset:	Digitally adjustable for each channel
Pulse shaping time:	Selectable, 1- 4 μs
Input referred noise:	< 200 e rms
Power consumption:	1500 mW nominal
Data readout:	Controlled by programmable token logic
Daisy chaining:	Up to 16 chips
Die size:	8.575 x 9.535 mm^2

III. ENERGY BINNING

A. XENA

The XENA IC ((**X**-ray **EN**ergy-binning **A**pplications)) has 32 detector readout channels; the block diagram for one channel is shown in Fig. 5. The key characteristics of XENA are given in Table IV. Its original target application was baggage screening, but it can likewise be used in medical imaging and other similar x-ray scanning methods.

Each XENA channel consists of a shaping amplifier with user-selectable shaping times between 250 ns and 4.0 µs, followed by a two-stage gain amplifier with adjustable gains and offsets. The amplifier input circuits accept signals of either polarity. The output signals from each channel are sent to five parallel comparators operating at different thresholds; the comparator outputs are connected to 16-bit digital counters. The 160 counters on each chip are read out by shifting a bit through a serial shift register, which causes the corresponding counter to be connected to the output bus.

A demonstration of the capabilities of the XENA IC is shown in Fig. 6 which plots the x-ray response of one pixel in a linear CZT array as a function of photon flux for each of the five energy bins.

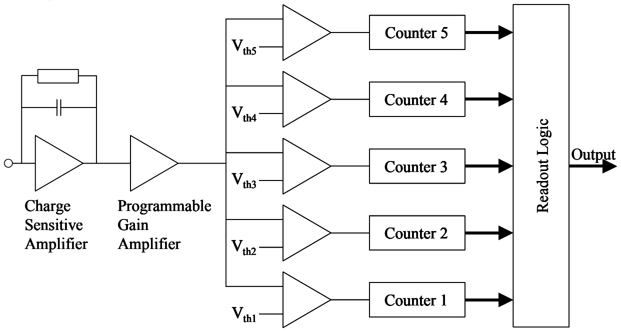

Fig. 5. Block diagram for one channel of the XENA IC.

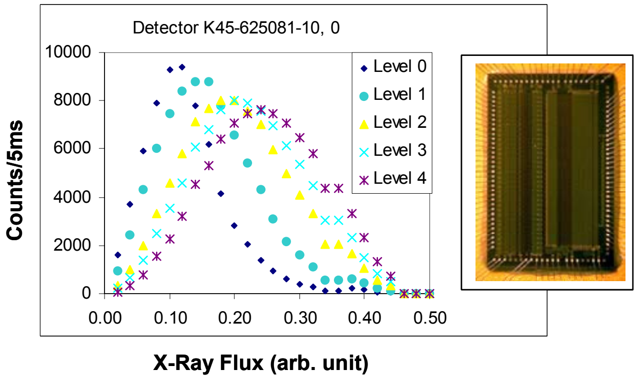

Fig. 6. Typical x-ray response curves obtained at room temperature for pixel number 0 in a 3 mm thick 2 x 16 pixel array CZT detector (eV PRODUCTS) with the XENA IC, as a function of x-ray flux; the tube voltage was fixed at160 kVp. Level 0 to Level 4 curves refer to the five bins defined by setting the five thresholds of each XENA channel at 0.2, 0.3, 0.4, 0.5, and 0.6 V, respectively, above baseline. Inset: XENA wire-bonded in CQFP package.

TABLE IV
KEY FEATURES OF THE XENA IC.

Number of Channels:	32 + two test channels
Data Readout:	160 counters read out sequentially over 16-bit parallel data bus
Readout Time:	≈ 20 µs for all 160 counters
Counter dynamic range:	16 bits
Count rate capability:	≈ 2 x 10^6 counts/second per channel
Energy bins per channel:	5
Comparator Levels:	Independent threshold voltages, ≈ 1.5-3.5 V, common to all channels
Gain and offset:	Digitally adjustable for each channel
Input loading capacitance:	3.5 pF optimum
Pulse shaping time:	Externally adjustable in two ranges, 250 ns to 4.0 µs
Input energy range:	≈ 20-300 keV
Input referred noise:	≈ 1000 e rms (4.5 keV for CZT)
Power consumption:	500 mW nominal

B. HILDA

The HILDA IC (**H**yperspectral **I**maging with **L**arge **D**etector **A**rrays) is a 16 x 16, 500mm pitch array of channels designed for high-rate photon counting and multiple-energy binning up to eight bands. Like the DANA, it is intended for use in flip-chip connection with a matching 2D detector pixel array. Such a 16 x 16, 500mm pitch CZT pixel array detector is currently in fabrication. The main application envisioned for this chip is munitions inspection.

Fig. 7 displays the HILDA IC layout and a picture of the fabricated die. The block diagram for a single channel of the HILDA is similar to that of the XENA (Fig.5) except that each channel has eight rather than five parallel comparators and counters. Table V summarizes the key features of HILDA.

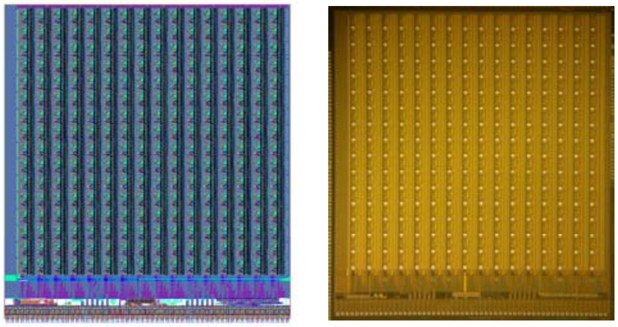

Fig. 7. Layout (left) and photograph (right) of the HILDA IC.

TABLE V
KEY FEATURES OF THE HILDA IC.

Number of channels:	16x16 matrix, 500μm pitch
Frond end:	Input amplifier feedback for continuous operation
Input energy range:	≈ 200 or 600 keV (CZT) maximum
Input polarity:	Negative
Count rate capability:	≈ 5 x10^6 counts/sec-channel
Energy bins per channel:	8
Gain and offset:	Digitally adjustable for each channel
Input loading capacitance:	0.5pF optimum
Charge collection:	50-100 ns
Input referred noise:	≈ 2200 e rms
Die size:	8.575 x 9.535 mm^2

IV. HIGH SPATIAL RESOLUTION IMAGING

A. MARY-2

Like the original MARY IC (**MA**mmog**R**aph**Y)**, MARY-2 is a solid-state pixel detector readout chip with a 192 x 384 array of 50 x 50 micron pixels operated in current mode with TDI CCD readout. The basic element of the array is a TDI group of eight pixels. Charge is integrated through eight shifts of position and then presented to an output buffer through a multiplexer and eventually to the external system. This accumulate-and-shift operation occurs continuously.

Fig. 8 shows a fabricated MARY die and the MARY-2 layout. The standard features of the MARY and MARY-2 include:

- TDI CCD Readout
- 16 Bit Dynamic Range
- Low Noise
- Internal and External Clock Drivers
- Fat Zero Test Input
- Overflow Control
- 24 Independent Readout Taps

The MARY-2 distinguishes itself from its predecessor via the following characteristics:

- Optimization for electron collection (CZT, Se)
- Availability of a staring mode option
- Fabrication in a current CCD process

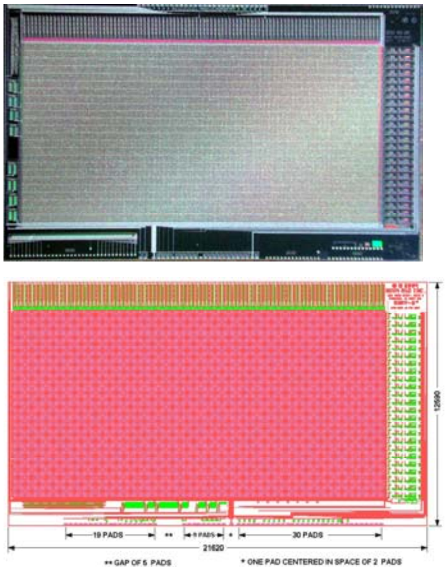

Fig. 8. Photograph of MARY (top) and layout of MARY-2 IC (bottom).

B. MARY-3

The MARY-3 is a 100 x 100 micron pixel version of the MARY-2 with a smaller 64 x 192 array size (Fig. 9). Its development was motivated by a desire to help spur progress in lower-cost bonding techniques for fine pixel arrays and to extend MARY applications from digital mammography to chest or full-body radiography and non-destructive inspection.

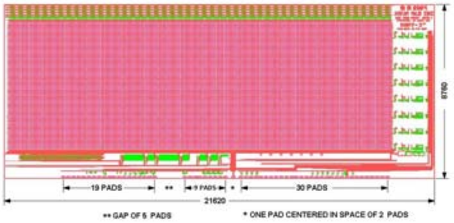

Fig. 8. Layout of MARY-3 IC.

V. SUMMARY

We have sought to broaden the usefulness of ASICs that we develop by expanding the features of a dedicated chip within its application development program. In parallel, we foresee that classes of IC designs can be defined and implemented according to application type. Direct support for the development of such "generic" readout IC solutions would benefit the radiation detector R&D community by reducing time and cost for prototyping new, advanced instrumentation concepts. The resulting generic designs can provide excellent starting points for more application-optimized and/or lower-cost versions of the readout chips.

The ICs described in this paper are either immediately available for evaluation (RENA-2 and XENA) or presently undergoing characterization (DANA, HILDA, MARY-2, MARY-3). NOVA welcomes all opportunities for collaboration to fully exploit the capabilities of its integrated readout electronics and hasten the development of emerging detector applications.

VI. ACKNOWLEDGMENT

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