New Readout Integrated Circuits for Position Sensitive Solid State Detectors

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***Abstract*—We have been developing custom multi channel mixed signal readout integrated circuits (ICs) for advanced position sensitive solid-state radiation detector arrays for applications ranging from x-ray astronomy and medical imaging to security and industrial inspection. Readout ICs are an integral part of position-sensitive semiconductor detectors for x-ray, gamma-ray and charged particle imaging. Different detector applications require custom IC, which is typically designed for a specific detector array. Therefore, it is important to develop generic ICs to meet a range of applications in different complementing fields. To achieve this aim NOVA has been developing generic ICs for different fields of applications, which embodies versatile and adaptable functions as well as selectable features. An overview of generic ICs developed at NOVA is presented here. Each chip described targets a complementing application field with versatile functions and features.**

I. Introduction

Applications of position-sensitive direct conversion solid-state radiation detectors have grown rapidly in recent years. The applications for these detectors are falling into six application fields: a) 1D Photon counting with high resolution individual photon energies acquired; b) 1D Fast photon counting with binning counts in several energy windows; c) 2D Photon counting with high resolution individual photon energies acquired; d) 2D Fast photon counting with binning counts in several energy window; e) 1D current integrating with current level output proportional to number of photons detected; and f) 2D current integrating with current level output proportional to number of photons detected. We present chips here developed by NOVA, which cover five of these general application fields.

The ICs (ASICs) developed at NOVA for these application fields are summarized in Table I.

II. RENA-2 IC

This IC is developed for the first application field listed above, 1D Photon counting with high resolution individual photon energies. RENA-2 chip (Fig. 1) is related to the earlier RENA IC (**R**eadout **E**lectronics for **N**uclear **A**pplications IC) [1] in functionality only. It embodies a completely new design with extensive features to render it versatile to meet the requirements of many different applications. (Please see NSS-2004 Conference Record R9-5 for a more detailed description and test results.)

Table I. A summary of the readout ICs developed to read out position sensitive solid state detectors for application in complementing fields.

Chip Name	Number of Channels			Energy Range or Key Signals (keV)	Energy Information	Target Detectors	Target Applicatons
	Linear	2D Array Matrix	μm Pitch				
RENA-2	36			< 10 to 1330	Photon counting w/full energy information	CZT, CdTe, Si, Ge, HgI2, GaAs, PbI2	Space physics, nuclear medicine, spectroscopy, security
DANA		16 x 16	500	1 to 150	Photon counting with full energy information	CZT, CdTe, Si, Ge	Space physics, nuclear medicine, spectroscopy, security
XENA	32			20 to 200	Photon counting, energy binning	CZT, CdTe, Si, GaAs, Se	Baggage screening, medical imaging, NDI
HILDA		16 x 16	500	10 to 200, or 40 to 600	Photon counting, energy binning	CZT, CdTe, Si, GaAs, Se	Munitions inspec., baggage screening, medical imaging, NDI and NDT
MARY-3		64 x 192	100	15 to 45; up to 150	Current mode	CZT, CdTe, Se, GaAs, Si	Digital mammography, chest or full-body radiography, NDI
MARY-2		192 x 384	50	15 to 45; up to 150	Current mode	CZT, CdTe, Se, GaAs, Si	Digital mammography, high-resolution NDI
FREDA	64			511	Photon energy	APD array w/ LSO, CsI, scintil. fiber	PET, SPECT, HEP & Astrophysics

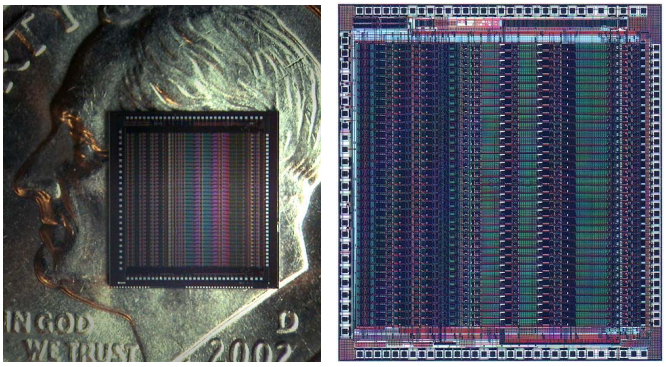

Fig. 1. On the left is a photograph of the RENA-2 IC placed on top of a dime to show its size. On the right is the actual silicon layout of the RENA-2 chip, implemented in the 0.5 micron AMI process.

RENA-2 IC features include the chip's low-noise performance, self-trigger capability and versatility in providing

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different peaking times, several readout modes and the daisy-chain option [2]. Specifically, the peaking times were made adjustable from about 0.4 to 40 microseconds, which makes the chip suitable for a wide range of detectors, from CdZnTe to HgI_2. The input amplifier was designed to tolerate leakage current so that detectors can be DC–coupled, thus eliminating the need to use capacitive AC coupling. The comparator thresholds are individually adjustable through an eight-bit DAC on each channel. This allows accurate and uniform threshold setting throughout the detector. Other innovative features include user-selectable dynamic range, fast trigger output for coincident event detection and the ability to provide channel-by-channel time difference information. The new chip also incorporates a pole zero cancellation circuit to handle large rates without significant pileup. Two important new features for space deployment are the ability to adjust power consumption by limiting the current flow to the input transistor and the radiation hardness inherent to the 0.5 micron CMOS process and augmented by special layout techniques. Four extra channels were moreover added to allow connecting the common electrode of a pixel detector to the same IC as its pixel electrodes. Further, the chip interface was streamlined and unnecessary connections were eliminated to enhance functionality. The key features of the RENA-2 IC are shown in Table II. The chip noise is low and the energy resolution is high as seen in the measured spectrum shown in Fig. 2.

Table II. Key design criteria and features of the RENA-2 IC.

Signal range:	Two full-scale ranges; 50 and 250 ke, selectable for each channel
Input polarity:	- or + (Selectable channel-by-channel)
Number of channels:	36 (extra channels to allow connection of common electrode)
Noise:	Minimize noise (112 e rms in lower signal range; 280 e rms in higher with a detector connected)
Noise optimization:	2ÊpF and 9 pF detector capacitance
DC leakage current:	Minimized & tolerant up to 25 nA leakage current
Power consumption:	< 5.8 mW per channel
Fast timing output:	Jitter minimized by use of fast shaping
Channel-channel time difference:	Implement
Power consumption:	Adjustable
Trigger comparator thresholds:	Individually adjustable by internal 8 Bit DACs for each channel
Peaking times:	0.36 to 38 microseconds in 16 steps
Fast count rates:	Using pole zero cancellation
Detector structure:	Heterogeneous or homogeneous
Key gamma signals:	14 keV, 60 keV, 141 keV, 511 keV, 662 keV, up to 1.33 MeV
System components:	Pipeline A/D converter, FPGA state machine controller, data FIFO
Interface:	Minimum pin count; support component count
Readout mode:	Maximum flexibility through hit register
Deadtime per event:	Minimized
Radiation tolerance:	Minimize effects by use of standard rad hard layout techniques to about 0.1 to 1 MRad

III. DANA IC

The DANA IC (**D**etector **A**rray for **N**uclear **A**pplications **I**ntegrated **C**ircuit) is a 16 x 16, 500mm pitch array of channels with a charge sensitive amplifier/shaper, trigger output and sparse readout intended for use in flip-chip connection with a spectroscopy-grade 2D detector pixel array. It is the 2D version of the RENA-2 chip, incorporating most of its functionality with much lower noise and higher energy resolution. The advantages of such a readout channel array include lower input capacitance and noise, finer pixel pitch, more compact sensor-readout assembly and ease of tiling array units into a large-area 2D array. On the other hand, its format entails the challenge of fitting complex circuitry within the unit cell area, developing the matching detector pixel array, and finding a solution for reliable and cost-effective IC-detector bonding.

Fig. 3 displays image of the DANA IC layout and

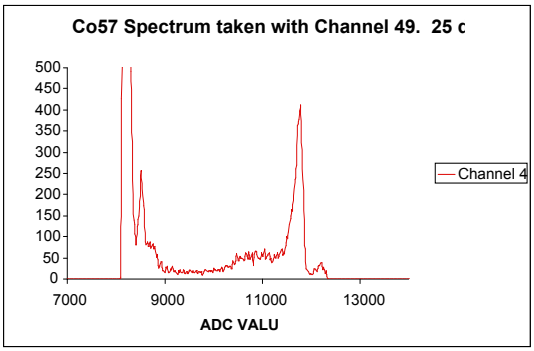

Fig. 2. RENA-2 IC Co-57 single pixel spectrum measured at room temperature using a 1.75 mm thick CdZnTe pixel array with 2 x 16 pixels at 1 x 1 mm^2 pixel pitch, fabricated by eV Products. The energy resolution is 3.7 keV FWHM @ 122 keV.

photograph of the fabricated die. The specifications of the DANA chip are summarized in Table III.

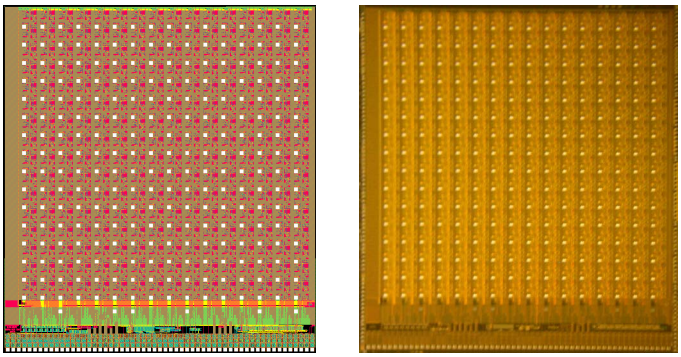

Fig. 3. Layout (left) and photograph (right) of the DANA IC.

Table III. Key features of the DANA IC.

Number of channels:	16x16 matrix, 500µm pitch
Front end:	Self-resetting charge sensitive amplifiers
Input energy range:	≈ 1-150 keV
Input polarity:	Positive and negative
Count rate capability:	> 400 $x10^3$ counts/sec, all channels in parallel
Gain and offset:	Digitally adjustable for each channel
Pulse shaping time:	Selectable, 1- 4 µs
Input referred noise:	≈ 30 e rms @ 0 pF input capacitance
Power consumption:	1500 mW nominal
Data readout:	Controlled by programmable token logic
Daisy chaining:	Up to 16 chips
Die size:	8.575 x 9.535 mm^2

IV. XENA IC

The XENA IC (**X**-ray **EN**ergy-binning **A**pplications) [3] has 32 detector readout channels. A photograph of the XENA IC is shown in Fig. 4. The XENA chip specifications are given in Table IV. Its original target application was baggage screening, but it can likewise be used in medical imaging and other similar x-ray scanning methods.

Each XENA channel consists of a shaping amplifier with user-selectable shaping times between 250 ns and 4.0 µs, followed by a two-stage gain amplifier with adjustable gains and offsets. The amplifier input circuits accept signals of either polarity. The output signals from each channel are sent to five parallel comparators operating at different thresholds; the comparator outputs are connected to 16-bit digital counters. The 160 counters on each chip are read out by shifting a bit through a serial shift register, which causes the corresponding counter to be connected to the output bus.

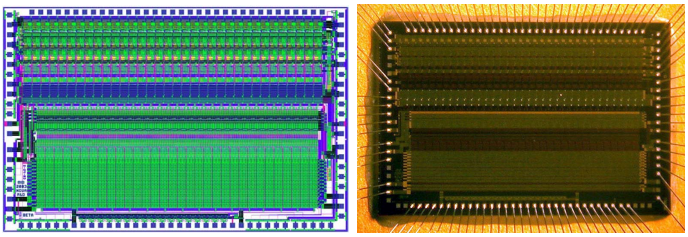

Fig. 4. Layout (left) and photograph (right) of the XENA IC.

Table IV. Specifications of the XENA IC.

Number of Channels:	32 + two test channels
Data Readout:	160 counters read out sequentially over 16-bit parallel data bus
Readout Time:	≈ 20 µs for all 160 counters
Counter dynamic range:	16 bits
Count rate capability:	≈ 2 x 10^6 counts/second per channel
Energy bins per channel:	5
Comparator Levels:	Independent threshold voltages, ≈ 1.5-3.5 V, common to all channels
Gain and offset:	Digitally adjustable for each channel
Input loading capacitance:	3.5 pF optimum
Pulse shaping time:	Externally adjustable in two ranges, 250 ns to 4.0 µs
Input energy range:	≈ 20-300 keV
Input referred noise:	≈ 100 e rms @ 0 pF input
Power consumption:	500 mW nominal

V. HILDA IC

The HILDA IC (**H**yperspectral **I**maging with **L**arge **D**etector **A**rrays) is a 16 x 16, 500mm pitch array of channels designed for high-rate photon counting and multiple-energy binning up to eight bands. Like the DANA, it is intended for use in flip-chip connection with a matching 2D detector pixel array. Such a 16 x 16, 500 µm pitch CZT pixel array detector is currently in fabrication. The main application envisioned for this chip is munitions inspection.

Fig. 5 displays the HILDA IC layout and a picture of the fabricated die. The HILDA chip is a 2D version of the XENA chip with improvements such as eight channels rather than five. Table V summarizes the key specifications of HILDA.

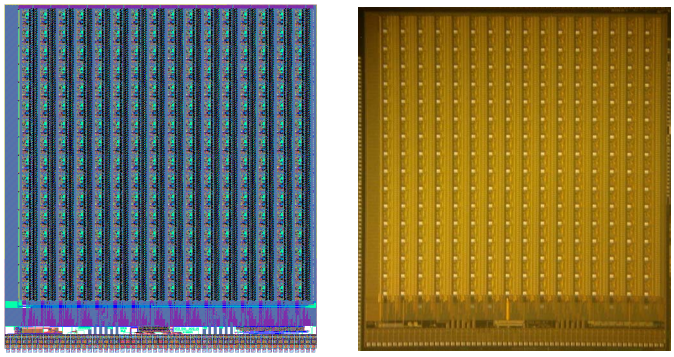

Fig. 5. Layout (left) and photograph (right) of the HILDA IC.

Table V. Specifications of the HILDA IC.

Number of channels:	16x16 matrix, 500µm pitch
Front end:	Input amplifier feedback for continuous operation
Input energy range:	≈ 200 or 600 keV (CZT) maximum
Input polarity:	Negative
Count rate capability:	≈ 5 x10^6 counts/sec-channel
Energy bins per channel:	8
Gain and offset:	Digitally adjustable for each channel
Input loading capacitance:	0.5 pF optimum
Charge collection:	50-100 ns
Input referred noise:	≈ 70 e rms @ 200 keV range
Die size:	8.575 x 9.535 mm^2

VI. MARY-2 IC

Like the original MARY IC (**MA**mmog**R**aph**Y**) [4], MARY-2 is a solid-state pixel detector readout chip with a 192x 384 array of 50 x 50 micron pixels operated in current mode with TDI CCD readout. The basic element of the array is a TDI group of eight pixels. Charge is integrated through eight shifts of position and then presented to an output buffer through a multiplexer and eventually to the external system. This accumulate-and-shift operation occurs continuously.

Fig. 6 shows a photograph of a fabricated MARY die and the MARY-2 layout. The standard features of the MARY and MARY-2 include:

- TDI CCD Readout
- 16 Bit Dynamic Range
- Low Noise
- Internal and External Clock Drivers
- Fat Zero Test Input
- Overflow Control
- 24 Independent Readout Taps

The MARY-2 distinguishes itself from its predecessor via the following characteristics:

- Optimization for electron collection (CZT, Se)

- Availability of a staring mode option
- Fabrication in a current CCD process

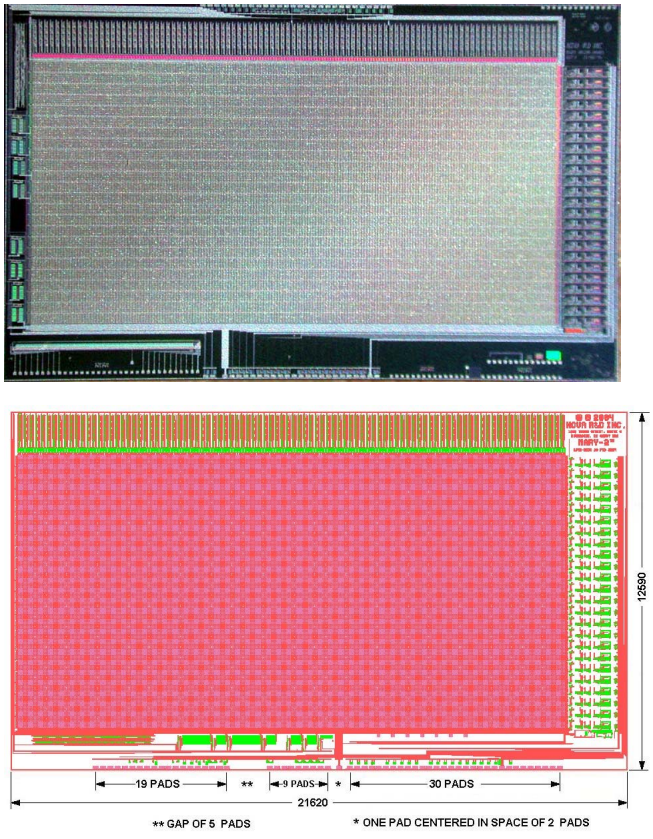

Fig. 6. Photograph of MARY IC (top) and layout of MARY-2 IC (bottom).

VII. MARY-3 IC

The MARY-3 is a 100 x 100 micron pixel version of the MARY-2 with a smaller 64 x 192 array size (Fig. 7). Its development was motivated by a desire to help spur progress in lower-cost bonding techniques for fine pixel arrays and to extend MARY applications from digital mammography to chest or full-body radiography, security such as baggage scanner and non-destructive inspection (NDI).

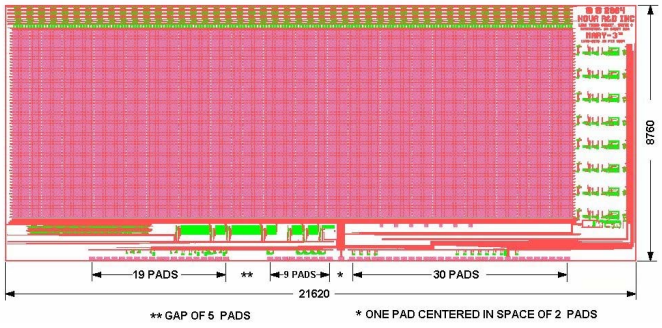

Fig. 7. Layout of MARY-3 IC.

VIII. SUMMARY

We have developed several generic ASICs for different application fields. These chips can be quickly optimized if necessary for a specific application, which are much less costly then development of a new IC.

The development of such "generic" readout IC solutions would benefit the radiation detector R&D community by reducing time and cost for prototyping new, advanced instrumentation concepts. It also allows the testing and characterization of the ICs to show feasibility and demonstrate applicability.

The resulting generic designs can provide excellent starting points for more application-optimized and/or lower-cost versions of the readout chips.

The ICs described in this paper are either immediately available for evaluation (RENA-2 and XENA) or presently undergoing characterization (DANA, HILDA, MARY-2, MARY-3). NOVA welcomes all opportunities for collaboration to fully exploit the capabilities of its integrated readout electronics and hasten the development of emerging detector applications.

NOVA is also developing ICs for other applications such as scintillator based detectors [5].

IX. ACKNOWLEDGMENT

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X. REFERENCES

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[5] This paper focuses on readout chips for direct conversion detectors. NOVA also has ICs designed for applications using scintillator crystals and PMTs or APDs. See for example, M. Clajus et al, "Compact detector modules for high resolution PET imaging with LYSO and avalanche photodiode arrays" *IEEE MIC conference record, M5-34, Rome, 2004.*