# Performance of an improved readout IC for multi-energy photon-counting x-ray detector arrays

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## ABSTRACT

We present the design and initial performance characterization of the XENA-2 readout IC for solid-state x-ray detector arrays. XENA-2 consists of 32 readout channels, each with charge-sensitive input amplifier, adjustable two-stage gain amplifier and five comparators with 16-bit pulse counters. Readout of the counters, over a 16-bit data bus, takes approximately 20 µs. Compared to the XENA chip, its predecessor, this new IC's main improvement is significantly reduced noise, which allows for lower comparator thresholds and increased count rates.

Keywords: radiation detector, pixel detector, CdZnTe, x-ray imaging, photon counting, multi-energy imaging

## 1. INTRODUCTION

Many x-ray imaging applications, including security screening of baggage, packages and vehicles; industrial imaging; and computed tomography (CT) for medical and non-medical applications require the detection of x-rays at high flux. In addition, an energy discrimination capability is found to be useful for an increasing range of these applications, to provide material identification capabilities, separate soft tissue and skeletal structures in medical imaging [1], reduce beam hardening artifacts in CT imaging [2], or reduce image blurring from low-energy scatter [3].

As a result, the interest in high-performance radiation detector systems suitable for high-flux multi-energy x-ray imaging has grown considerably. In the late 1990s, NOVA developed the FESA (Front-end Electronics for Spectroscopy Applications) IC [4] for use in the multi-energy x-ray detector system [5] designed for the ABIS project (Automated Baggage Inspection System) sponsored by the US Army ARDEC and the Department of Agriculture. Since then, other groups have presented IC designs and detector systems that utilize the same readout channel architecture consisting of a charge-sensitive input amplifier followed by one or more gain and/or shaping amplifiers that feed into several parallel comparators and counters; see, for example, [6] and [7].

At NOVA, the FESA design was followed by the XENA (X-ray ENergy-binning Applications) IC [8], which used an improved amplifier design and addressed power distribution issues to achieve significant noise reduction. The FESA power distribution issues had prevented the use of some features, most notably the fine adjustment of the comparator thresholds, which became fully usable in XENA. In addition to these considerable performance improvements, the design was implemented in a more modern 0.5 µm process.

The XENA IC, however, exhibited some residual noise issues that affected mostly the lowest-numbered channels, where the noise was noticeably higher than in the other channels. In order to address these issues, we recently developed a further improved version of XENA, called XENA-2. At the same time, we implemented other improvements, such as increasing the resolution of the offset and threshold adjustment DACs by two bits each. This paper presents the design of the XENA-2 IC and discusses first, preliminary test results from this chip.

## 2. DESIGN OF THE XENA-2 IC

Like the original XENA IC [8], XENA-2 has 32 fully functional detector readout channels plus two amplifier-only channels at the top and bottom ends of the channel that are intended to mitigate performance non-uniformities near the edges of the die and can be used for test purposes. A simplified block diagram for one full channel is shown in Figure 1.

Each XENA-2 channel consists of a charge-sensitive input amplifier with user-selectable shaping times between ~100 ns and 4.0 µs, followed by a two-stage gain amplifier with adjustable gains and offsets. The output signals from each channel are sent to five parallel comparators operating at different thresholds; the comparator outputs are in turn connected to 16-bit digital counters. The 160 counters on each chip are read out by shifting a bit through a serial shift

Hard X-Ray, Gamma-Ray, and Neutron Detector Physics X, edited by Arnold Burger, Larry A. Franks, Ralph B. James,
Proc. of SPIE Vol. 7079, 707911, (2008) · 0277-786X/08/$18 · doi: 10.1117/12.795607

register, which causes the corresponding counter to be connected to the 16-bit output bus; the readout can be done in about 20 µs. Table I summarizes key characteristics of XENA-2.

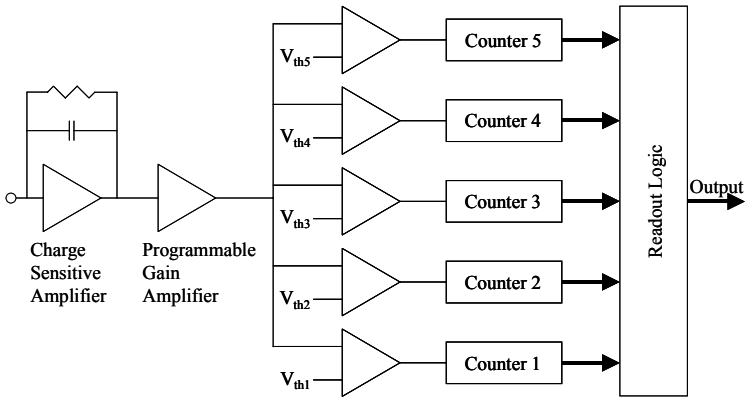


**Figure 1:** Simplified block diagram of a readout channel on the XENA-2 IC.

**Table I:** Key features of the XENA-2 IC.

| | |
|---|---|
| Number of channels | 32 + two test channels |
| Energy bins per channel | 5 |
| Counter dynamic range | 16 bits |
| Count rate capability | $\approx 2 \times 10^6$ counts/second per channel |
| Readout time | ≈ 20 µs for all 160 counters |
| Gain and offset | Digitally adjustable for each channel |
| Input loading capacitance | 2 – 3 pF optimum |
| Pulse shaping time | Externally adjustable in two ranges, 100 ns to 4.0 µs |
| Input energy ranges | 200 keV nominal and 800 keV nom. |
| Power consumption | ~ 500 mW nominal |

The charge-sensitive amplifier's input circuits are optimized for a detector capacitance of 2 to 3 pF and accept signals of either polarity. Two signal ranges, 200 keV and 800 keV nominal, can be selected by switching the capacitors in the feedback path. The resistive feedback is provided by a transconductance amplifier whose transconductance is controlled by an externally supplied bias current, Itau. This allows us to continuously vary the output pulse width between approximately 100 ns and 2.5 µs in the 200 keV range, when measured at one tenth the peak amplitude, and ~250 ns to 4 µs in the 800 keV range.

The two gain stages that follow the input amplifier have adjustable offset (in the second stage) and gain to compensate for pixel-to-pixel differences of the detector signal and leakage current and for process variations that affect the uniformity of the channel response. The offset is controlled by a 10-bit R-2R DAC. The DAC step size is proportional to an externally supplied reference voltage; the proportionality constant is approximately $1.3 \times 10^{-3}$. The gain adjustment has five bits, two in the first gain stage for a coarse adjustment, and three with a finer step size in the second. The range of nominal gain values from the two stages combined is 6.1 to 29.7.

The threshold voltages for the five comparators are common to all 32 channels and are supplied externally. A four-bit DAC at each comparator can be used to shift the effective threshold in steps of approximately 2 mV and thus compensate for process variations in the voltage offsets of the comparator amplifiers. The comparator hysteresis is typically 50 mV but can be varied by adjusting an external bias current.

The counters record all pulses whose amplitude exceeds the corresponding comparator threshold. They are read out sequentially by channel, and by counter within each channel. To reduce the readout dead time in cases where only one counter per channel is needed, XENA-2 can be configured to read only the first counter in each channel.

For test purposes, XENA-2 provides a test signal input that can be AC-coupled to any combination of channels, including the amplifier-only channels; the coupling capacitance is 75 fF nominally. Additionally, the amplifier output of any one of these 34 channels at a time can be connected to a buffered analog monitor output.

Figure 2 shows the layout of the chip. The detector input pads are located on the left edge of the die and the input amplifier, gain amplifiers, comparators, and counters are arranged left to right in each channel Compared to XENA, the channel length has increased to accommodate added offset and comparator DAC bits, resulting in an almost square overall layout. The die size is 5.9 mm × 5.7 mm. The IC is fabricated in a 0.6 µm process and packaged in a 144-pin CQFP.

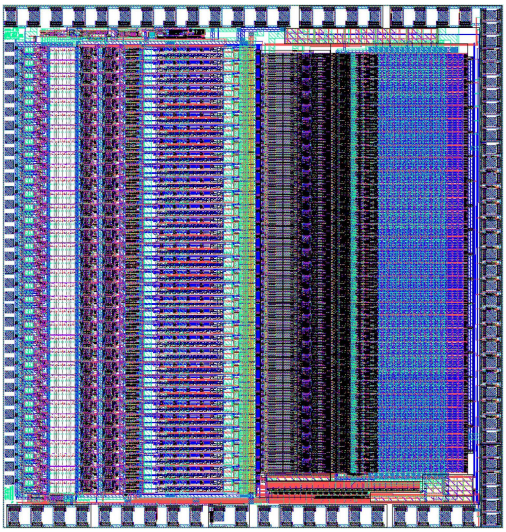

**Figure 2:** Layout of the XENA-2 IC.

## 3. XENA-2 PERFORMANCE

To test the performance of XENA-2, we placed it in a test system that had been custom-designed for the original XENA IC and is equipped with a commercial test socket. The test board provides the power regulation, bias supplies and threshold DACs for the chip and features an FPGA to control the IC configuration and readout. Connectors for a test pulse signal, the chip's analog signal output, and for a 2×16-pixel CZT detector array connecting to the XENA-2 inputs are also provided. The test system is controlled from a PC via a proprietary PCI I/O board. Adapting the system for use with XENA-2 only required changing a few bias resistors on the test board.

In the following paragraphs, we discuss preliminary results from our first tests of XENA-2, starting with the amplifier section and then moving on to the comparators and counters. We conclude this section by presenting first results obtained with a CZT pixel detector read out by XENA-2.

The linearity of the analog offset DACs was verified by connecting the analog monitor output to a GPIB-controlled digital voltmeter, without any input from a detector or the test signal input, and measuring the DC baseline level for different channels as a function of the DAC value. Figure 3 shows an example of such a linearity measurement, displaying the baseline voltage as a function of DAC value for all 34 channels, including the analog-only test channels, of one of the XENA-2 ICs. The excellent linearity of the DAC response and consistency of the slopes seen in the figure are typical for the overall performance we encountered. Only three of the nearly 650 channels on 19 chips for which we have measured this response so far had visually noticeable nonlinearities. We used linear least-squares fits for a quantitative characterization of the linearity; the $R^2$ value was above 0.999 for all channels except those three, with a median of 0.99998. For the channels on any given chip, the slopes from the fits agreed within a standard deviation of

less than 0.7%. Between chips, the standard deviation was 2.4%. With the value for the DAC reference voltage that we used, the DAC step size was typically between 1.20 and 1.25 mV.

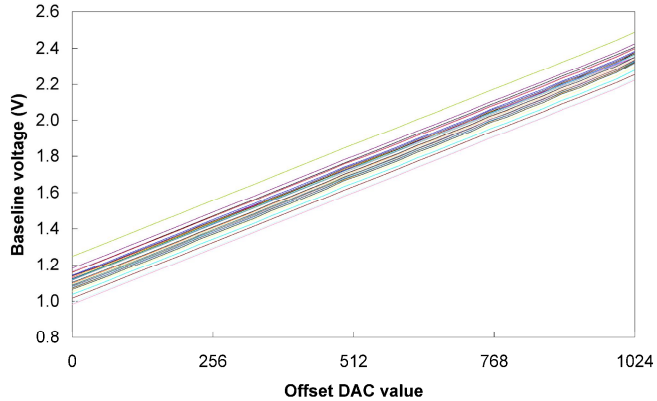


**Figure 3:** Offset linearity measurement for all channels of one of the XENA-2 ICs tested.

Figure 4 shows an oscilloscope screen shot of the amplifier response to a negative-going 5 fC test pulse input, as seen at the analog test output. The amplifier gain was set to a nominal value of 11.9 and the feedback control current Itau to 10 µA. The fast, low-energy input amplifier range was used for all measurements discussed in this paper. The vertical scale in Figure 4 is 200 mV/div, the horizontal scale is 80 ns/div.

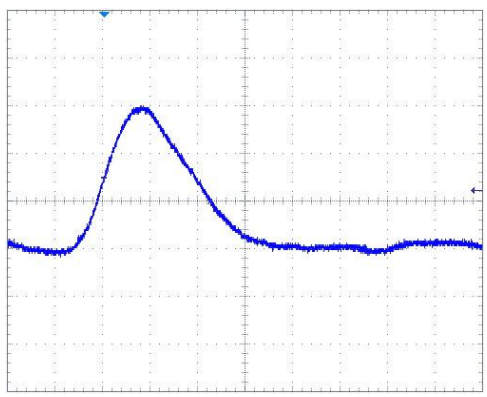

**Figure 4:** Pulse shape in response to a 5 fC test pulse input. Itau was set to 10 µA and the nominal amplifier gain was 11.9.

To measure the signal amplitude at the amplifier output in response to periodic test pulse inputs, we used one of the comparators and associated counters. We varied the comparator's threshold voltage and measured the count rates as a function of this voltage. As long as the threshold was clearly below the pulse amplitude, all pulses were counted; when the threshold was well above the amplitude, no counts were recorded. The width of the transition region was controlled by the signal noise, which pushed some pulses high enough to cross the threshold while others didn't; the comparator's hysteresis prevented it from triggering multiple times on the same pulse. This threshold dependence of the count rate is demonstrated by the blue diamonds in Figure 5 for a 5 fC input amplitude (assuming that the AC coupling capacitance at the test input is close to its nominal value of 75 fF). It can be fitted with a cumulative normal distribution, indicated by the solid line. The mean and sigma obtained from the fit represent the amplitude and rms noise level, respectively of the amplifier signal. We repeated these measurements for different test pulse amplitudes and plotted the output vs. input pulse heights after subtracting the signal baseline voltage, which for these measurements was set to 1.75 V. An example of this is shown in Figure 6 for one of the channels for which we performed these measurements. Error bars indicating the measured noise level are smaller than the symbol size. The minimum input amplitude of 1.875 fC was limited by the range of the pulse generator used in the measurement. As expected, the relationship is reproduced quite well by a straight-line fit, which is indicated by the dashed line in Figure 6. The slope of this line is the combined gain of the amplifier chain, consisting of the input amplifier and the two gain stages; it amounts to 64 mV/fC in this case. The deviation of the intercept from zero is consistent with the measured rms noise.

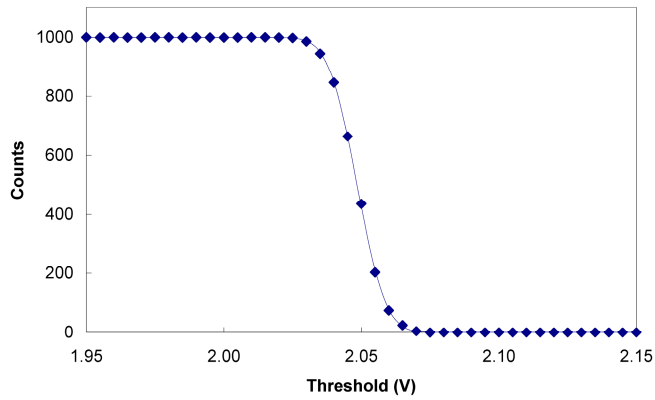


**Figure 5:** Number of pulses counted during a fixed time period in response to a periodic test signal, as a function of the comparator threshold voltage in the vicinity of the pulse amplitude. The diamonds represent measured data; the solid curve is from a fit with a cumulative normal distribution.

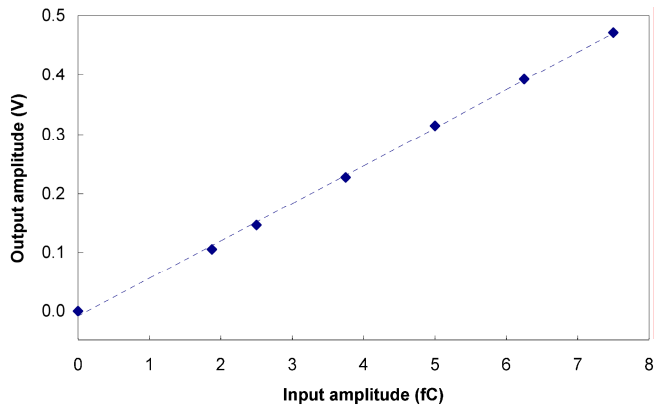


**Figure 6:** Measured amplitude at the amplifier output as a function of input pulse height. The dashed line is a linear fit to the data.

The data shown in Figure 6 were obtained with the nominal gain of the gain amplifiers set to 11.9. In order to verify the circuit simulation results for the amplifier gain, we repeated the measurements at different gain settings spanning the entire adjustment range. The results are summarized in Figure 7(a) and show a linear relationship between measured and nominal gains. Moreover, an extrapolation of the fit to the data, which is indicated by the dashed line in Figure 7(a), comes out close to the origin, within a nominal gain range of ±1. In other words, the measured data are consistent with the results of the circuit simulations, except for a common scale factor, which we can identify with the gain of the charge-sensitive input amplifier. For the channels that we tested, the input amplifier gain varied between 4.5 and 5.0 mV/fC.

We can use the results of these gain measurements to convert the noise values that we obtained from fits like the one shown in Figure 5 to an input-referred level. When we do this and average the results over the different channels and input pulse amplitudes at any given gain setting, we get the data points shown in Figure 7(b). The error bars represent the standard deviations of the data obtained at each gain setting. The input-referred rms noise varies only minimally as a function of gain; the overall average is indicated by the dashed line in Figure 7(b) and amounts to 0.13 fC – just over 800 electrons, or between 3.65 and 3.7 keV in CZT. The noise is consistent over all channels, demonstrating the expected improvement compared to the XENA design.

The gain of the input amplifier depends, of course, on its feedback resistance, which is in turn determined by the control current Itau; for the measurements discussed above, Itau was set to 5 µA. In order to determine the dependence of the gain on Itau, we repeated similar measurements as the ones discussed above at different values of this current. For the time being, however, we limited these measurements to a single input amplitude (5 fC) and a single gain setting (11.9 nominal) of the gain amplifier stages. This approach implicitly assumes that the linearity of the gain amplifiers is not significantly affected by variations in Itau. Figure 8(a) shows the results for Itau values ranging from 1 µA to 32 µA. By

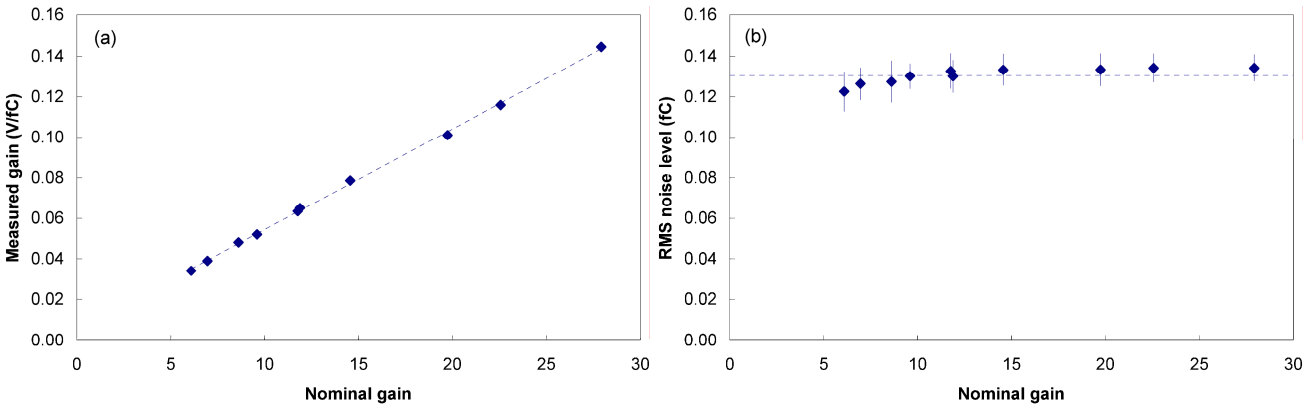


**Figure 7:** (a) Measured amplifier gain as a function of the nominal gain setting of the two gain stages. The dashed line indicates a straight-line fit to the data. (b) Measured input-referred rms noise level as a function of the nominal gain setting of the two gain stages. The error bars indicate the variation of the values over the different input amplitudes and over different channels. The dashed line represents the average of the data points shown.

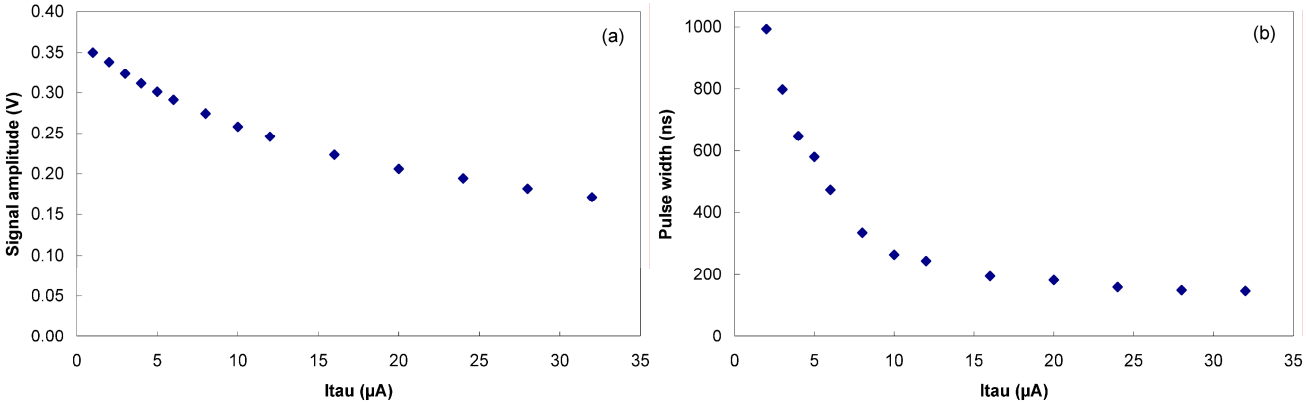


**Figure 8:** (a)Signal amplitudes measured at the amplifier output in response to a 5 fC input, for different values of Itau and a fixed gain setting of the gain stage. (b) Amplifier output pulse width, measured at 10% of the peak amplitude, for different values of Itau.

normalizing these amplitudes to the results obtained at Itau = 5 μA, we estimate that the input amplifier gain varies between 0.54 and 0.58 mV/fC at Itau = 1 μA, and between 0.26 and 0.28 mV/fC at 32 μA

At the same time, we connected the XENA-2 IC's analog test output to a digital storage oscilloscope and acquired sample pulse shapes, like the one shown in Figure 4, for the different Itau values. These samples were then analyzed to determine the pulse widths at 10% of the peak amplitude. The results are shown in Figure 8(b); the data point at Itau = 1 μA, where the pulse width is 2.56 μs, was left off the graph to avoid compressing the vertical scale for the remaining data points too much.

As discussed in Section 2, the XENA-2 comparators are equipped with four-bit DACs to compensate for variations of their switching points for a given threshold voltage. To test the functionality of these DACs, we re-measured the amplifier response curves shown in Figure 5, which had been acquired with a comparator DAC setting of 0, with different DAC values and for each of the chip's five comparator levels. The results were again fitted with cumulative normal distributions to determine the shift in the amplitude measurement that resulted from the threshold offset introduced by the DAC. As shown in Figure 9(a), the results vary linearly with the DAC values; the step sizes determined from straight-line fits to the data range from 1.8 to 2.1 mV. The resulting adjustment range is sufficient to compensate for variations between comparators in the same channel. Figure 9(b) shows the input-referred noise levels corresponding to the data of Figure 9(a); it demonstrates that the DAC setting does not affect the noise and that there are no significant noise differences between comparator levels.

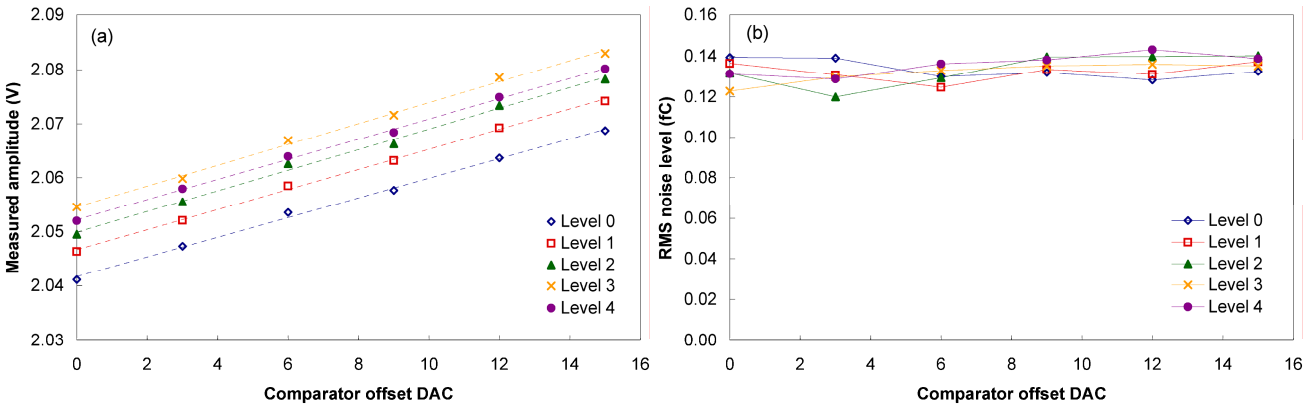


**Figure 9:** (a) Change in the apparent pulse amplitude as a function of the comparator DAC value for all five comparators of one XENA-2 channel. The correspondence between the plot symbols and the comparator levels is indicated in the legend. The dashed lines show linear fits to each of the five data sets. (b) Input-referred noise levels associated with the data shown in (a).

After adjusting the DACs to even out the switching voltages for all five comparators in each channel, we connected a 3 mm thick 2×16-pixel CZT detector array with 1 mm pixel pitch, manufactured by eV PRODUCTS, to the XENA-2 inputs. The test system was placed in the beam of NOVA's Pantak HF-160 x-ray generator, which was set to a tube voltage of 140 kVp. After providing –600 V bias to the detector, the signal baselines were adjusted to 1.75 V again to make up for the shift that resulted from the detector leakage currents. We set the amplifier gains to 11.9 (nom.) and the five comparator threshold voltages to 1.8, 1.85, 1.9, 1.95 and 2.0 V, respectively, and measured the detector count rates for the five threshold levels as a function of the x-ray tube current. These measurements were repeated for four different values of Itau – 5.0, 7.5, 10.0, and 12.5 µA. As expected, the maximum count rate that the detector and readout can process increases with Itau; this is shown in Figure 10(a). The peak count rate measured at 12.5 µA amounts to approximately 1.1 million counts per second. Further increases can be expected as Itau is raised all the way to 32 µA. Figure 10(b) shows the response in all five comparator levels at a Itau = 12.5 µA.

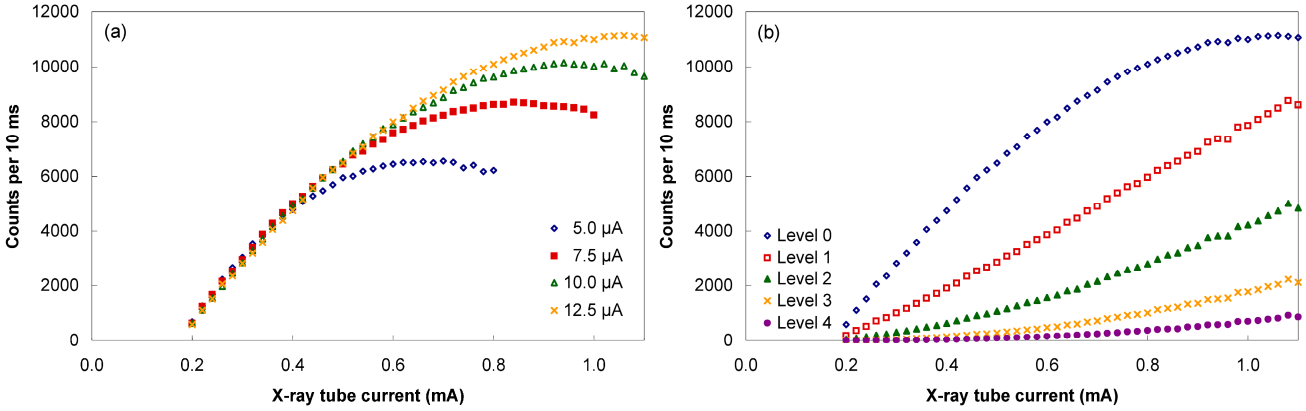


**Figure 10:** (a) Count rate measured for the lowest comparator level of one of the detector pixels as a function of. x-ray tube current. The data were acquired for Itau current settings of 5 (diamonds), 7.5 (squares), 10 (triangles), and 12.5 µA. (b) Count rate vs. x-ray tube current for the five comparator levels of the same detector pixel as shown in (a). Itau was set to 12.5 µA for this measurement.

## 4. SUMMARY

We have presented the design and preliminary test results of the XENA-2 IC, which has recently been developed by NOVA R&D, Inc. for use in high-flux, multi-energy x-ray imaging. In its characterization so far, the new chip has exhibited performance characteristics that are consistent with circuit simulations and provide the expected improvement over the earlier XENA design.

## ACKNOWLEDGMENTS

We thank David Ward and Gary Kline for their contributions to the XENA-2 design.

## REFERENCES


[1] Alvarez, R.E., and Macovski, A., "Energy-selective reconstruction in x-ray computerised tomography," Phys. Med. Biol. 21(5), 733-744 (1976).

[2] Kowase, K., and Ogawa, K., "Photon counting x-ray CT system with a semiconductor detector," 2006 IEEE Nucl. Sci. Symp. Conf. Rec., Vol. 5, p. 3119-3123.

[3] Willson, P., Clajus, M., Tümer, T.O., Visser, G., and Cajipe, V., "Imaging using energy discriminating radiation detector array," AIP Conf. Proc. 680, 913-920 (2003).

[4] Clajus, M.,. Tümer, T.O, Visser, G.J., Yin, S., Willson, P.D., and Maeding, D.G., "Front-End Electronics for Spectroscopy Applications (FESA) IC," 2000 IEEE Nucl. Sci. Symp. Conf. Rec., Vol. 2, p. 9/227-9/229.

[5] Clajus, M., et al., "Scanned x-ray images from a linear CdZnTe pad array with monolithic readout electronics," Proc. SPIE 4141, 274-280 (2000).

[6] Tomita, Y., Shirayanagi, Y., Matsui, S., Aoki, T., and Hatanaka, Y., "X-ray color scanner with multiple energy discrimination capability," Proc. SPIE 5922, 40-47 (2005).

[7] De Geronimo, G., Dragone, A., Grosholz, J., O'Connor, P., and Vernon, E., "ASIC with Multiple Energy Discrimination for High-Rate Photon Counting Applications," IEEE Trans. Nucl. Sci. 54(2), 303-312 (2007).

[8] Cajipe, V.B., Calderwood, R.F., Clajus, M., Grattan, B., Hayakawa, S., Jayaraman, R., Tumer, T.O., and Yossifor, O., "Multi-energy x-ray imaging with linear CZT pixel arrays and integrated electronics," 2004 IEEE Nucl. Sci. Symp. Conf. Rec., Vol. 7, p. 4548-4551.