Improved Readout IC for Multi-Energy X-Ray Imaging with Linear CZT Pixel Arrays

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Abstract—We have developed a new, improved version of the XENA (X-ray ENergy-binning Applications) readout IC for solid-state x-ray detector arrays, which we call XENA-2. This IC consists of 32 readout channels, each with charge-sensitive input amplifier, two-stage gain amplifier, and five comparators followed by 16-bit pulse counters. The resistive feedback of the input amplifier is provided by a transconductance circuit with continuously variable, user-controlled transconductance, which allows the amplifier's shaping time to be varied between 100 to 150 ns and 4 μs. Two input amplitude ranges, 7 fC and 30 fC nominal (200 keV and 800 keV, respectively, for Cadmium Zinc Telluride), can be selected by switching different capacitors into the feedback path. The gain amplifier design includes a five-bit gain adjustment and a ten-bit R-2R offset DAC. The five comparator threshold voltages are supplied externally and are common to all channels; digitally controlled threshold adjustments at each comparator allow to compensate for process variations. Readout of the counters, over a 16-bit data bus, takes approximately 20 μs. Two additional analog-only channels (that is, without the comparators and counters) are provided, one at each end of the channel array; they are used for test purposes and to improve the uniformity of the full channels. Compared to XENA, this new IC's main improvement is significantly reduced noise, which allows for lower comparator thresholds and increased count rates. XENA-2 is fully pin-compatible with XENA and replaces it as the readout IC used in NOVA's NEXIS detector system.

I. INTRODUCTION

MANY x-ray imaging applications, including security screening of baggage, packages and vehicles; industrial imaging; and computed tomography (CT) for medical and non-medical applications require the detection of x-rays at high flux. In addition, an energy discrimination capability is found to be useful for an increasing range of these applications, to provide material identification capabilities, separate soft tissue and skeletal structures in medical imaging [1], reduce beam hardening artifacts in CT imaging [2], or reduce image blurring from low-energy scatter [3].

As a result, the interest in high-performance radiation detector systems suitable for high-flux multi-energy x-ray imaging has grown considerably. In the late 1990s, NOVA developed the FESA (Front-end Electronics for Spectroscopy Applications) IC [4] for use in the multi-energy x-ray detector system [5] designed for the ABIS project (Automated Baggage Inspection System) sponsored by the US Army

ARDEC and the Department of Agriculture. Since then, other groups have presented IC designs and detector systems that utilize the same readout channel architecture consisting of a charge-sensitive input amplifier followed by one or more gain and/or shaping amplifiers that feed into several parallel comparators and counters; see, for example, [6] and [7].

At NOVA, the FESA design was followed by the XENA (X-ray ENergy-binning Applications) IC [8], which used an improved amplifier design and addressed power distribution problems to achieve significant noise reduction. The FESA power distribution problems had prevented the use of some features, most notably the fine adjustment of the comparator thresholds, which became fully usable in XENA. In addition to these considerable performance improvements, the XENA design was implemented in a more modern 0.5 μm process.

The XENA IC, however, exhibited some residual noise that affected mostly the lowest-numbered channels, where the noise was noticeably higher than in the other channels. In order to address this issue, we recently developed a further improved version of XENA, called XENA-2. At the same time, we implemented other improvements, such as increasing by two bits each the resolution of the digital-to-analog converters (DACs) used to adjust analog offsets and comparator thresholds. This paper presents the design of the XENA-2 IC and discusses test results from this chip.

II. DESIGN OF THE XENA-2 IC

Like the original XENA IC [8], XENA-2 has 32 fully functional detector readout channels plus two amplifier-only channels at the top and bottom ends of the channel array that are intended to mitigate performance non-uniformities near the edges of the die and can be used for test purposes. Fig. 1 shows a simplified block diagram for one full channel.

Each XENA-2 channel consists of a charge-sensitive input amplifier with user-selectable shaping times between ~100 ns and 4.0 μs, followed by a two-stage gain amplifier with adjustable gains and offsets. The output signals from each channel are sent to five parallel comparators operating at different thresholds; the comparator outputs are in turn connected to 16-bit digital counters. The 160 counters on each chip are read out by shifting a bit through a serial shift register, which causes the corresponding counter to be connected to the 16-bit output bus. The readout can be completed in about 20 μs. Table I summarizes key characteristics of XENA-2.
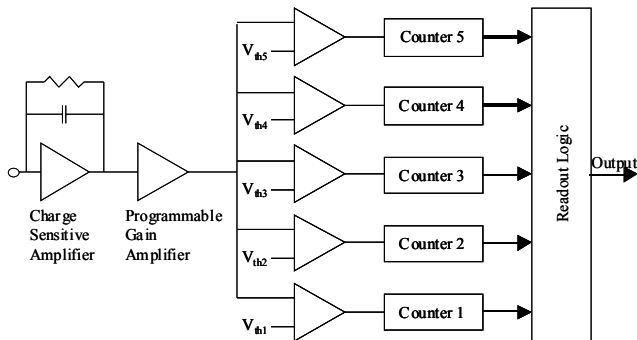
Fig. 1. Simplified block diagram of a readout channel on the XENA-2 IC.

Table I. Key features of the XENA-2 IC.

Number of channels	32, plus two test channels
Energy bins	Five per channel
Counter depth	16 bits
Count rate capability	$\approx 2 \times 10^6$ counts per second per channel
Readout time	≈ 20 µs for all 160 counters
Gain and offset	Digitally adjustable for each channel
Input capacitance	Optimized for 2-3 pF
Input energy ranges	Two ranges, 200 keV and 800 keV nominal

The charge-sensitive amplifier's input circuits are optimized for a detector capacitance of 2 to 3 pF and accept signals of either polarity. Two signal ranges, 200 keV and 800 keV nominal, can be selected by switching the capacitors in the feedback path; this selection is common to all channels. The resistive feedback is provided by a transconductance amplifier whose transconductance is controlled by an externally supplied bias current, labeled Itau. This allows us to continuously vary the output pulse width, measured at one tenth the peak amplitude, between approximately 100 ns and 2.5 µs in the 200 keV range, and ~250 ns to 4 µs in the 800 keV range.

The two gain stages that follow the input amplifier have adjustable offset (in the second stage) and gain to compensate for pixel-to-pixel differences of the detector signal and leakage current and for process variations that affect the uniformity of the channel response. The offset is controlled by a 10-bit R-2R DAC. The DAC step size is proportional to an externally supplied reference voltage; the proportionality constant is approximately 1.3×10^{-3}. The gain adjustment has five bits, two in the first gain stage for a coarse adjustment with a nominal range from 2.9 to 9.4, and three with a finer step size, ranging from 2.1 to 3.0, in the second. The range of nominal gain values from the two stages combined is 6.1 to 27.9.

The threshold voltages for each of the five comparators are common to all 32 channels and are supplied externally. A four-bit DAC at each comparator can be used to shift the effective threshold in steps of approximately 2 mV and thus compensate for process variations in the offset voltages of the comparator amplifiers. The comparator hysteresis is typically 50 mV but can be varied by adjusting an external bias current. To accommodate both positive and negative signal polarities, the sign of the hysteresis can be selected through a global polarity configuration bit.

The counters record all pulses whose amplitude exceeds the corresponding comparator threshold. They are read out sequentially by channel, and by counter within each channel. In cases where only one counter per channel is needed, XENA-2 can be configured to read only the first counter in each channel, reducing the readout dead time by a factor five.

For test purposes, XENA-2 provides a test signal input that can be AC-coupled to any combination of channels, including the amplifier-only channels; the nominal value of the coupling capacitance in each channel is 75 fF. Additionally, the amplifier output of any one of these 34 channels at a time can be connected to a buffered analog monitor output.

The XENA-2 configuration is controlled by 35 individually addressable 44-bit registers – one per channel and one global register – that are loaded through a common serial shift register.

Fig. 2 shows the layout of the chip. The detector input pads are located on the left edge of the die, and the input amplifier, gain amplifiers, comparators, and counters are arranged left to right in each channel. Compared to XENA, the channel length has increased to accommodate added offset and comparator DAC bits, resulting in an almost square overall layout. The die size is 5.9 mm × 5.7 mm. The IC is fabricated in a 0.6 µm process and packaged in a 144-pin CQFP.
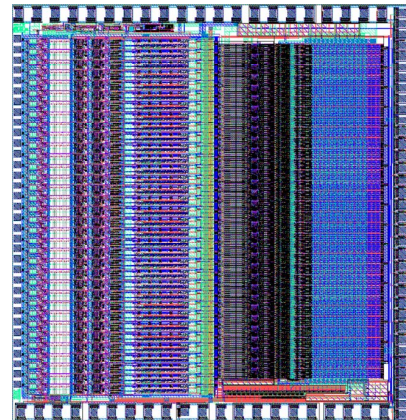

Fig. 2. Layout of the XENA-2 IC.

III. XENA-2 PERFORMANCE

To test the performance of XENA-2, we placed it in a test system that had been custom-designed for the original XENA IC and is equipped with a commercial off-the-shelf test socket. The test board provides the power regulation, bias supplies and threshold DACs for the chip and features a field-programmable gate array (FPGA) to control the IC configuration and readout. Connectors for a test pulse signal,

the chip's analog signal output, and for a 2×16-pixel Cadmium Zinc Telluride (CZT) detector array connecting to the XENA-2 inputs are also provided. The test system is controlled from a PC via a proprietary PCI I/O board. Because XENA-2 was designed to be pin-compatible with XENA, we were able to adapt the test system for use with the new chip by changing a few bias resistors on the test board and updating the control software to accommodate the additional configuration bits. Fig. 3 shows a photograph of the XENA test board.

Fig. 3. Photograph of the XENA test board. A CZT detector array is installed on the left side of the board, next to the IC socket.

The linearity of the analog offset DACs was verified by connecting the analog monitor output to a computer-controlled digital voltmeter, without any input from a detector or the test signal input, and measuring the DC baseline level for different channels as a function of the DAC value. Fig. 4 shows an example of such a linearity measurement, displaying the baseline voltage as a function of DAC value for half the channels of one of the XENA-2 ICs. The excellent linearity of the DAC response and consistency of the slopes seen in the figure are typical for the overall performance we encountered. Out of just over 130 ICs that we tested, 16 had one or more channels with offset nonlinearities that caused us to reject the chip. In all but two of these cases, the underlying problem was either a single nonfunctioning DAC bit, or the entire DAC (or the analog test output) did not respond to configuration changes. We used linear least-squares fits for a quantitative characterization of the data; the median R^2 value for those parts that passed the offset linearity test was 0.99998. For the channels on any given chip, the slopes from the fits agreed within a standard deviation of 1.0% or less; between chips, the standard deviation was 2.8%. With the value for the DAC reference voltage that we used, the DAC step size was typically between 1.20 and 1.25 mV.
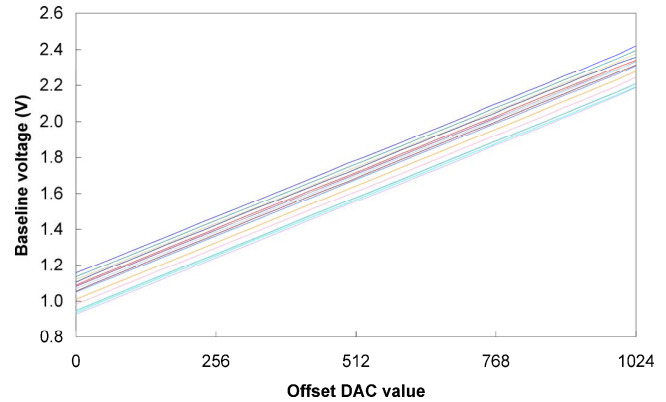

Fig. 4. Offset linearity measurement for the odd-numbered channels of one of the XENA-2 ICs tested.

Fig. 5 shows oscilloscope traces of the amplifier response to a negative-going test pulse input, as seen at the analog test output. The step size of the test signal was 67 mV, which corresponds to 5 fC if we assume that the AC coupling capacitance at the test input is close to its nominal value of 75 fF. The input amplifier was set to the 200 keV range, the gain amplifiers to a nominal gain of 11.9, and the feedback control current Itau ranged from 8 µA to 24 µA.
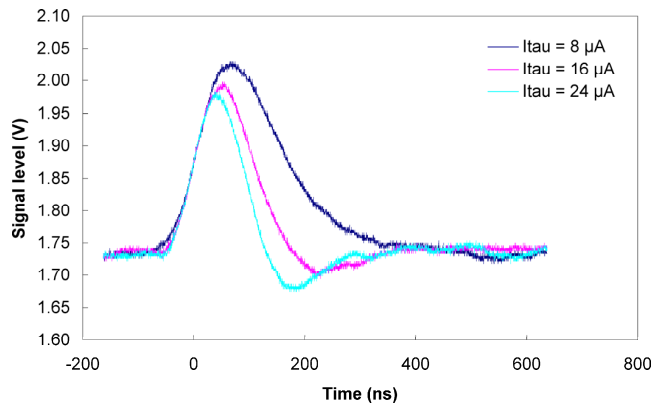

Fig. 5. Pulse shapes in response to a 5 fC test pulse input. Itau was set to 8, 16, and 24 µA, respectively and the nominal amplifier gain was 11.9.

To measure the signal amplitude at the amplifier output in response to periodic test pulse inputs, we used one of the comparators and associated counters. We varied the comparator's threshold voltage and measured the count rates as a function of this voltage. As long as the threshold was clearly below the pulse amplitude, all pulses were counted; when the threshold was well above the amplitude, no counts were recorded. The width of the transition region was controlled by the signal noise, which pushed some pulses high enough to cross the threshold while others were not able to do so. This threshold dependence of the count rate is demonstrated by the data in Fig. 6 for an input amplitude of 5 fC. It can be fitted with a normal distribution, indicated by the solid curve. The mean and sigma obtained from the fit correspond to the amplitude and rms noise level, respectively, of the amplifier signal. We repeated these measurements for different test pulse amplitudes and plotted the output

amplitude as a function of input pulse height. Examples of this are shown in Fig. 7 for both input energy ranges for one of the channels for which we performed these measurements. Error bars indicating the measured noise level would be smaller than the symbol size. As expected, the relationships are reproduced quite well by straight-line fits, which are also shown in Fig. 7. The slopes of these lines are the combined gain of the amplifier chain, consisting of the input amplifier and the two gain stages. For the fits shown in Fig. 7, they amount to 65 mV/fC in the 200 keV range and 17.6 mV/fC in the 800 keV range. Within the uncertainty given by the rms noise, the value of the intercept in either case is consistent with the baseline voltage set prior to the measurement.
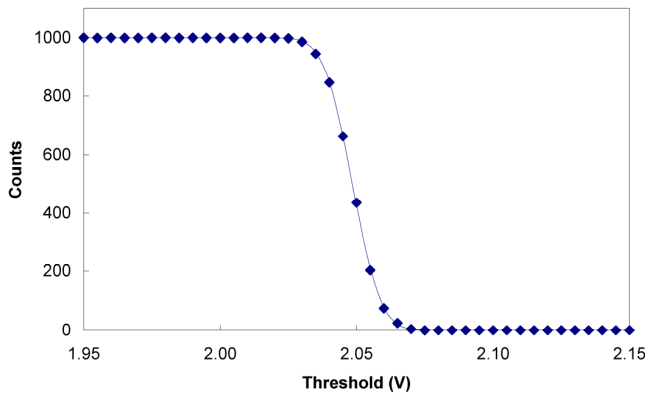

Fig. 6. Number of pulses counted during a fixed time period in response to a periodic test signal, as a function of the comparator threshold voltage in the vicinity of the pulse amplitude. The diamonds represent measured data; the solid curve is from a fit with a normal distribution.
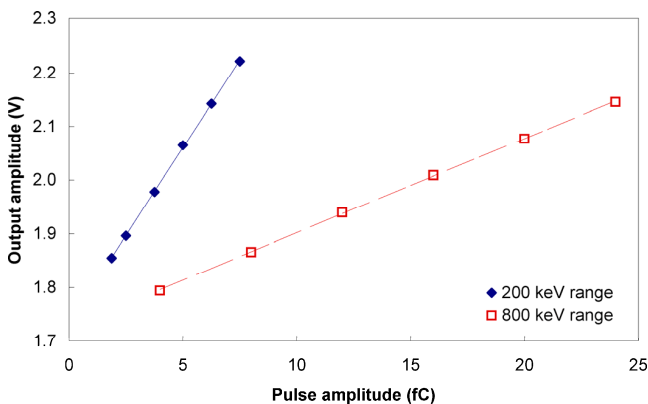

Fig. 7. Measured amplitude at the amplifier output as a function of input pulse height. Data for the input amplifier's 200 keV range are indicated by solid diamonds, those for the 800 keV range by open squares. The solid and dashed lines represent linear fits to the data.

In order to verify the nominal values for the amplifier gain, we repeated the measurements shown in Fig. 7 at different gain settings spanning the entire adjustment range. The results are summarized in Fig. 8, again for both input amplifier gain ranges. Linear fits, indicated by the solid and dashed lines in Fig. 8, show good proportionality between measured and nominal gains. This result allows us to identify the proportionality factor with the gain of the charge-sensitive input amplifier. For the channels that we tested, this input

amplifier gain varied between 4.5 and 5.0 mV/fC in the 200 keV range, and between 1.29 and 1.35 mV/fC in the 800 keV range.

The rms noise values that we obtain from fits like the one shown in Fig. 6 do not vary significantly between different channels, demonstrating the expected improvement compared to the XENA design. The noise level is also stable as a function of the input pulse height and, when converted to an input-referred level, as a function of the gain amplifier setting. The average input-referred noise amounts to 0.13 fC – just over 800 electrons, or between 3.65 and 3.7 keV in CZT – in the input amplifier's 200 keV range, and to 0.21 fC (1330 electrons, 6.0 keV) in the 800 keV range.
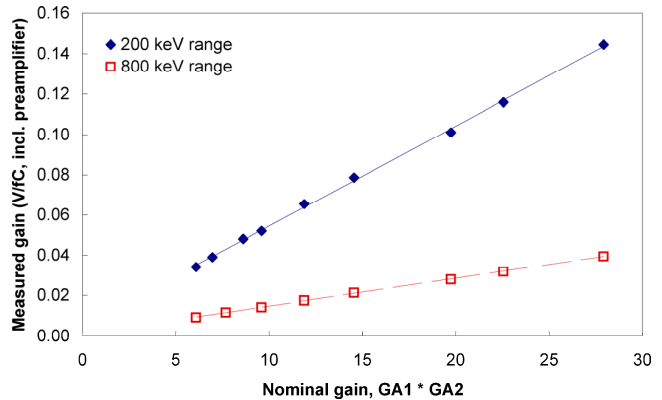

Fig. 8. Measured amplifier gain as a function of the nominal gain setting of the two gain stages for the 200 keV (diamonds) and 800 keV gain ranges (squares) of the input amplifier. The solid and dashed lines, respectively, indicate linear fits to the data.

The gain of the input amplifier depends, of course, on its feedback resistance, which is in turn determined by the control current Itau. For the measurements discussed above, Itau was set to 5 μA. In order to determine the dependence of the gain on Itau, we repeated our amplitude measurements at different values of this current. For the time being, however, we limited these measurements to the 200 keV input amplifier range, to a single input amplitude (5 fC), and to a single gain setting (11.9 nominal) of the gain amplifier stages. The latter two restrictions implicitly assume that the linearity of the gain amplifier response is not significantly affected by changing Itau. Fig. 9 shows the results for Itau values ranging from 1 μA to 32 μA. By normalizing the amplitudes to the results obtained at Itau = 5 μA, we estimate that the input amplifier gain varies between 5.4 and 5.8 mV/fC at Itau = 1 μA, and between 2.6 and 2.8 mV/fC at 32 μA.

At the same time, we connected the chip's analog test output to a digital storage oscilloscope and recorded sample pulse shapes for the different Itau values, some of which are shown in Fig. 5. We then analyzed these samples to determine the pulse widths at 10% of the peak amplitude. The results are shown in Fig. 10; the data point at Itau = 1 μA, where the pulse width is 2.56 μs, was left off the graph to avoid compressing the vertical scale for the remaining data points too much.
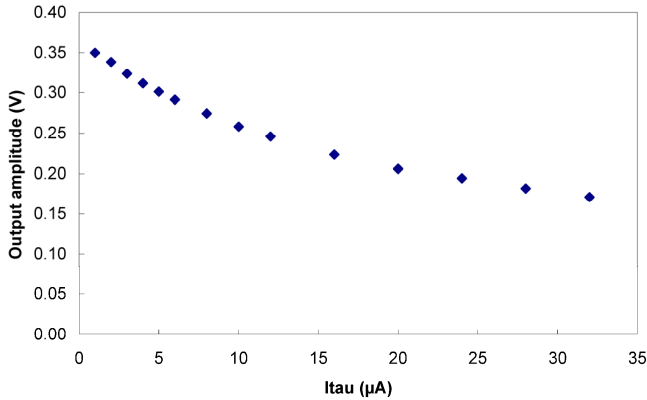
Fig. 9. Signal amplitudes measured at the analog test output in response to a 5 fC input, for different values of Itau and a fixed gain setting of the gain stage. The input amplifier was set to the 200 keV range.
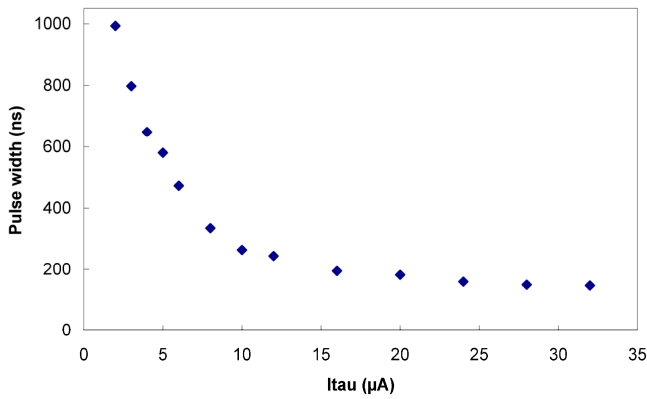

Fig. 10. Amplifier output pulse width, measured at 10% of the peak amplitude, for different values of Itau. The input amplifier was set to the 200 keV range.

To determine the value of the comparator hysteresis, we acquired the amplifier response curves shown in Fig. 6 for both values of the chip's polarization bit. All other configuration settings being equal, this change caused a horizontal offset between the curves that was equal to the amount of the hysteresis. The result of this measurement is summarized in Fig. 11 for the level 0 comparators of the chip being tested. The average value of the hysteresis for all 160 comparators, which is indicated by the dashed line, is 47.7 mV, with a standard deviation of 1.0 mV and no systematic differences between the levels.

As discussed in Section II, the XENA-2 comparators are equipped with four-bit DACs to compensate for threshold offsets. To test the functionality of these DACs, we re-measured the amplifier response curves, which had been acquired with a comparator DAC setting of 0, with different DAC values and for each of the chip's five comparator levels. The results were again fitted with normal distributions to determine the shift in the measured amplitudes that resulted from the threshold offset introduced by the DAC. As shown in Fig. 12, the results vary linearly with the DAC values. The step sizes determined from straight-line fits to the data range from 1.8 to 2.1 mV, resulting in an adjustment range that is sufficient to compensate for variations between comparators in

the same channel. Our measurements also showed that rms noise levels do not vary significantly between comparator levels or as a function of the comparator DAC setting.
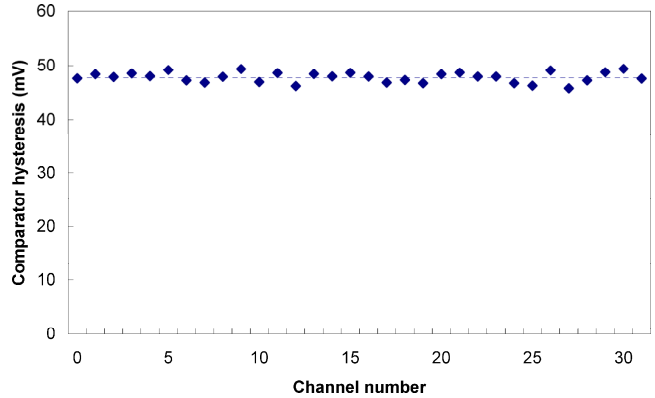

Fig. 11. Measured comparator hysteresis for comparator level 0 in all 32 full channels of a XENA-2 IC. The dashed line indicates the average value.
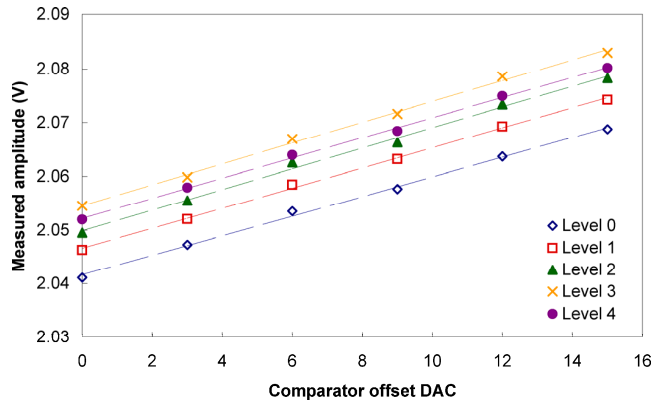

Fig. 12. Change in the measured pulse amplitude as a function of the comparator DAC value for all five comparators of one XENA-2 channel. The correspondence between the plot symbols and the comparator levels is indicated in the legend. The dashed lines show linear fits to each of the five data sets.

Based on these results, we adjusted the DACs to match the switching voltages for all five comparators in each channel. We then connected a 3 mm thick 2×16-pixel CZT detector array with 1 mm pixel pitch, manufactured by eV PRODUCTS, to the XENA-2 inputs. The test system was placed in the beam of NOVA's Pantak HF-160 x-ray generator, which was set to a tube voltage of 140 kVp and a current of 0.22 mA. After providing 600 V bias to the detector, the signal baselines were readjusted to 1.75 V to make up for the shift that resulted from the detector leakage currents, and the amplifier gains were set to a nominal value of 11.9. The input amplifiers were set to the 200 keV range and Itau to 5 µA. We used two of the comparators in each channel to form a window discriminator by setting their thresholds approximately 6 mV apart and subtracting the counts obtained at the higher threshold from those for the lower threshold. By simultaneously varying the two thresholds of this window discriminator, we were able to measure the spectrum of the x-ray generator. Fig. 13 shows the spectrum obtained from one of the detector pixels.
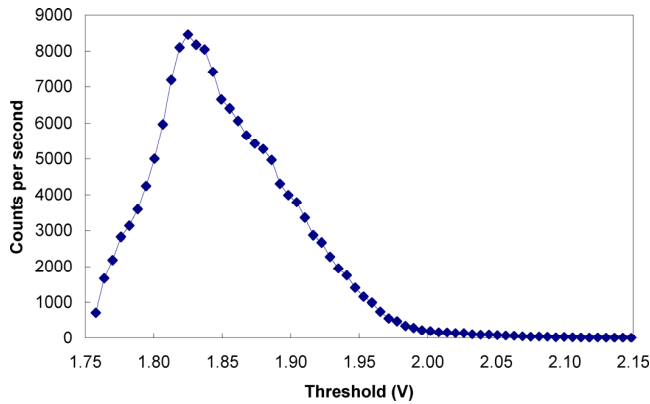
Fig. 13. Spectrum of NOVA's x-ray generator, acquired by a pixel of the CZT detector connected to the XENA-2 inputs. The generator was operated at 140 kVp.

Finally, we set the five comparator threshold voltages to 1.8, 1.85, 1.9, 1.95 and 2.0 V, respectively, and measured the detector count rates for the five comparator levels as a function of the x-ray tube current. These measurements were repeated for four different values of Itau – 5.0, 7.5, 10.0, and 12.5 µA. As expected, the maximum count rate that the detector and readout can process increases with Itau; this is shown in Fig. 14. The peak count rate measured at 12.5 µA amounts to approximately 1.1 million counts per second. Further increases can be expected as Itau is raised all the way to 32 µA. Fig. 15 shows the response in all five comparator levels at Itau = 12.5 µA.
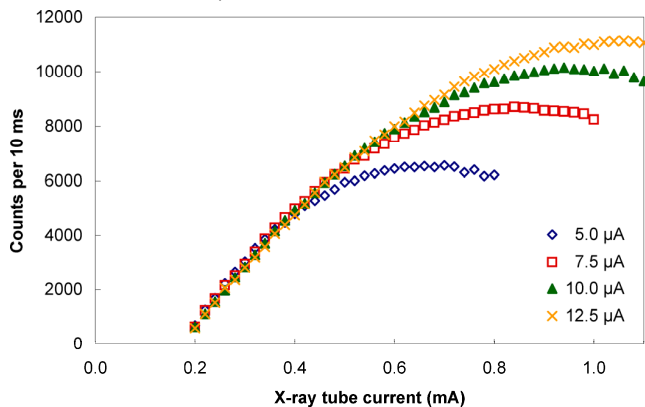

Fig. 14. Count rate measured for the lowest comparator level of one of the detector pixels as a function of. x-ray tube current. The data were acquired for Itau currents between 5 and 12.5 µA, as indicated in the legend.
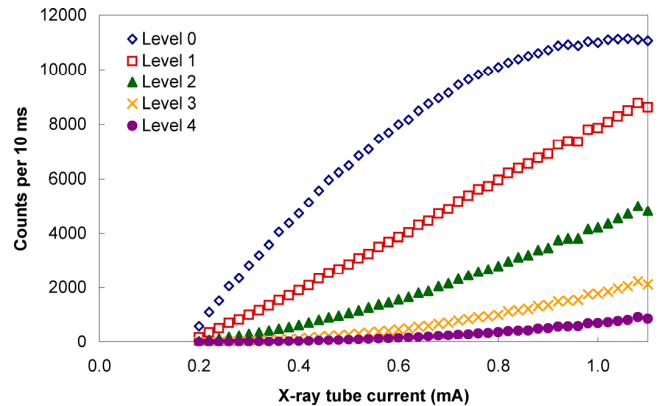

Fig. 15. Count rate vs. x-ray tube current for the five comparator levels of the same detector pixel as shown in Fig. 14. Itau was set to 12.5 µA for this measurement.

IV. SUMMARY

We have presented the design and test results of the XENA-2 IC, which has recently been developed by NOVA R&D, Inc. for use in high-flux, multi-energy x-ray imaging. In its characterization so far, the new chip has exhibited performance characteristics that are consistent with circuit simulations and provide the expected improvement over the earlier XENA design

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