Multi-Channel Front-End Readout IC for Position Sensitive Solid-State Detectors

Tümay O. Tümer, Victoria B. Cajipe, Martin Clajus, Satoshi Hayakawa and Alexander Volkovskii, Member, IEEE

Abstract—A multi-channel front-end readout IC is developed for position sensitive solid-state detectors. It is called RENA-3. It has 36 low noise channels. Each channel has externally selectable input polarity. The channel inputs are optimized for 2 or 9 pF detector capacitance, which is externally selectable. It also has selectable dual energy range, 56K and 338K electrons (250 keV and 1.5 Mev for CZT, respectively). A fast trigger output is provided applications that require timing. A novel circuit produces arrival time difference measurement for each channel. It is developed to serve as front-end readout electronics for a variety of position-sensitive solid-state semiconductor detectors such as CdZnTe, Si, GaAs and HgI2. It also has flexibility for use with other types of solid-state detectors such as Ge, Se, PbI2 and CdTe in a multichannel strip or pixel geometry to detect and image x-rays and gamma-rays with energies up to 1.3 MeV. Also a novel register circuit and process allows nearest neighbor readout capability for pixel detectors. Combination of RENA-3 chips with a variety of semiconductor detectors would be suitable for numerous applications in astrophysics, nuclear physics, nuclear medicine, security and industrial imaging. Some possible applications include gamma camera, SPECT, small animal PET and SPECT, nuclear source detection and spectroscopy, space x-ray and gamma-ray astronomy missions, NDE and NDI.

I. INTRODUCTION

The RENA-2 and RENA-3 integrated circuits (ICs) (Fig. 1) are related to the earlier RENA IC (Readout Electronics for Nuclear Applications IC) [1] in basic functionality only. They embody a completely new design with extensive new features to render it versatile to meet the requirements of many different applications.

The RENA-3 IC is recently developed and it is identical in functionality and layout of RENA-2 [2]. We have made improvements to some of the circuits and the layout of the RENA-3 chip to make it more stable. The RENA-2/-3 IC features include the chip’s low-noise performance, self-trigger capability and versatility in providing different peaking times, several readout modes and the daisy-chain option [2]. Specifically, the peaking times were made adjustable from about 0.4 to 40 microseconds, which makes the chip suitable for a wide range of detectors, from Silicon, CdZnTe, Ge to HgI2. The input amplifier was designed to tolerate leakage current so that detectors can be DC–coupled, thus eliminating the need to use capacitive AC coupling. The comparator thresholds are individually adjustable through an eight-bit DAC on each channel. This allows accurate and uniform threshold setting throughout the detector. Other innovative features include user-selectable dynamic range, fast trigger output for coincident event detection and the ability to provide channel-by-channel time difference information. The new chip also incorporates a pole zero cancellation circuit to handle large rates without significant pileup. Two important new features for space deployment are the ability to adjust power consumption by limiting the current flow to the input transistor and the radiation hardness inherent to the 0.5 micron CMOS process and augmented by special layout techniques. Four extra channels were moreover added to allow connecting the common electrode of a pixel detector to the same IC as its pixel electrodes. Further, the chip interface was streamlined and unnecessary connections were eliminated to enhance functionality.

II. RENA-3 IC DESCRIPTION

RENA-3 is a 36-channel mixed signal ASIC chip with low-noise self-resetting charge sensitive preamplifiers at the input of each channel (Fig. 2). The extra channels are built in to allow connection to the common electrodes of solid state pixel detectors. Each channel has two individually selectable dynamic ranges for wide energy range applications (≤9 fC and ≥54 fC). The chip is designed for low noise (simulations show 45 to 120 e rms input referred noise for each range @ 0 pF input capacitance.) The inputs are single-ended to improve noise performance. Channel-by-channel selection of negative or positive input polarity allows signal detection from both the anode and cathode on the same detector. A sparse readout mode is available for reading out only the channel, which contain data. Another option is an on-chip generalized neighbor readout mode, which can be applied for both strip and 2-D pixel array detectors. RENA-3 features low power

Fig. 1. On the left is a photograph of the RENA-2 IC placed on top of a dime to show its size. On the right is the actual silicon layout of the RENA-2 chip, implemented in the 0.5 micron AMI process. RENA-3 is very similar with only some circuit improvements.

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T. O. Tümer, V. B. Cajipe, M. Clajus, S. Hayakawa and A. Volkovskii are with NOVA R&D, Inc., Riverside, CA 92507 USA (telephone: 951-781-7332, first author e-mail: tumay.tumer@novarad.com).

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operation \( \leq 5.8 \, \text{mW/Ch} \) for space based astrophysics applications. Power consumption is adjustable. Also full or partial power down is available on a channel-by-channel basis. The chip is optimized for two input capacitances (2 pF & 9 pF selectable channel-by-channel).

![Fig. 2. RENA-2/-3 IC single channel block diagram showing all the analog circuitry and some of the control system.](image)

One of the most important features of RENA-3 is its self-resetting charge-sensitive input preamplifier (Fig. 2). The self-resetting function restores the increase in pedestal produced by the detector leakage current and eliminates the need for AC coupled connection between the detector channel and the input amplifier. Therefore, RENA-3 has been designed with built-in tolerance for detector leakage current (< \pm 5 \, \text{nA}) and it can be DC coupled to most position sensitive solid state detectors.

RENA-3 also has selectable peaking times from 0.36 to 38\( \mu \text{s} \) in 16 steps. This extensive range of peaking times allows RENA-3 to be used for many different kinds of solid state detectors, from fast silicon pixel and strip detectors to much slower Ge and HgI\(_2\) detectors. It also has a high resolution and accurate peak and hold circuit for carrying out high energy resolution spectroscopy with ease.

The RENA-3 chip is designed to have a self-trigger output capability using a comparator (Fig. 3). The self-trigger output is especially important for nuclear and radiography applications where the incident photon arrives at random and its arrival time is not known.

Some applications require accurate (low jitter) fast timing signals for coincident imaging such as positron emission tomography (PET) and double Compton scatter detectors. RENA-3 is designed to accommodate such applications by incorporating a fast low jitter shaping and comparator circuit on each channel (Fig. 3). This circuit produces a fast timing trigger output, which is separate from the slow event trigger output. The slow trigger output provides accurate pulse-height discrimination for event triggers and must be used for recording an event, and the fast trigger should be used in conjunction with the event trigger for coincidence determination. Another interesting functionality built into the RENA-3 chip is the time stamp circuit at each channel (Figs. 2 & 3). This circuit utilizes user-supplied time-variable signals to produce data on channel-to-channel pulse arrival time difference. This feature can be useful if information on the arrival time differences for multiple simultaneous events is required.

RENA-3 also has a third high threshold comparator (Fig. 3) that triggers whenever the input signal exceeds the dynamic range of the amplifiers. In RENA-3 provisions were made to enable fine tuning and compensation for channel-to-channel and chip-to-chip fabrication variations. For example, an adjustment of comparator thresholds for each channel is achieved by using a DAC at each comparator.

The RENA-3 chip may be used in fast photon counting applications. To achieve smooth fast photon counting at short peaking times, a pole zero cancellation circuit, which reduces pulse pileup for high input signal rates was incorporated into the IC. Up to eight RENA-3 chips can be wired together to be read out as a single chip with 288 channels. This feature will be useful for large channel low rate applications. The chip has a low noise differential analog output to preserve its low noise high energy resolution capability.

![Fig. 3. Schematic diagram of the RENA-2/-3 ASIC. Only one channel (Channel k) is shown; connections to adjacent channels are indicated where applicable; the slow and fast signals are shown multiplexed.](image)

### III. RENA-3 SPECIFICATIONS AND APPLICATIONS

The key RENA-3 key design features and general specifications are listed in Table I. Table I also shows the many new features RENA-3 chip has to make it a versatile and flexible integrated circuit to address the needs of many different applications.

RENA-3 can therefore be used for many different applications in medical, industrial, NDI and security fields. A long list of target detector applications is available. Most of the applications are for imaging x-rays and gamma rays. However,
the chip can be used with any detector or system that produces charge pulses in the time frame of picoseconds to microseconds.

RENA-3 is also developed with many interesting and different features so that it can be tested and investigated for different applications. Once the investigation is complete and the chip is found that it will work, then it can be optimized for each application and unneeded circuits can be also taken out.

RENA-3 IC Test System

A RENA-3 Evaluation System has been developed to test the new IC. Fig. 4 displays a photograph of the RENA-3 IC.

V. RENA-3 IC Diagnostic Features

Every channel of the RENA-3 has a test pulse input (707 mV step injects full scale signal = 53 fC). The test pulses can be turned on and off individually for each channel. This capability allows for testing the chip without a detector. RENA-3 also has several diagnostic modes. For example, the follower mode bypasses the peak hold circuit and connects the shaper output directly to the output of the channel. The force-enable mode provides the capability of continuous monitoring of the peak detector or shaper output of any externally selected channel. There are also buffered probe pads provided at important points on channels 0 and 35 of the RENA-3 chip for testing and monitoring of the critical sections of the analog circuitry.

VI. RENA-3 IC Preliminary Test Results

The RENA-2/-3 IC noise was simulated during the design phase. The results show that at 0 pF detector input capacitance the input referred noise can be as low as 45 and 60 e rms for low and high dynamic range modes, respectively. The power dissipation for each channel was also simulated. The results show ≈ 5.8 mW per channel maximum power dissipation.

Tests were performed on the fabricated RENA-3 prototype chips (Fig. 5) using the above-described evaluation system board (Fig. 4).

Noise measurements were carried out on RENA-2 for different detector input capacitances plotted for the two externally selectable detector capacitance ranges, 2 and 9 pF. The preliminary measurements show that 0 pF detector capacitance results in ≈ 140 and 150 e rms noise at room temperature [2], respectively, for the two detector capacitance ranges. This measurement will be repeated for RENA-3.
Fig. 6 shows a RENA-3 linearity measurement. The output pulse heights were measured with an oscilloscope set for continuous average with a weight of 1:15. The input pulse was put through a 1pF capacitor mounted directly on the detector input to the IC channel. The RENA-3 chip was configured for maximum channel gain. The red vertical line near the center shows the design limit for the lower energy (higher gain) dynamic range, 200 keV.

![Fig. 6. RENA-3 IC linearity measurement.](image)

X-ray spectra were also acquired simultaneously on multiple channels of the prototype RENA-3 IC. Fig. 7 shows a Co-57 single pixel spectrum measured at room temperature using a 1.75 mm thick CdZnTe pixel array with 2 x 16 pixels at 1 x 1 mm² pixel pitch (Fig. 9), fabricated by eV Products. The energy resolution is about 5 keV FWHM at 122 keV.

![Fig. 7. The RENA-3 IC Co-57 single pixel spectrum measured at room temperature using a 1.75 mm thick CdZnTe pixel array with 2 x 16 pixels at 1 x 1 mm² pixel pitch, fabricated by eV Products. The spectrum is corrected by using time of arrival (time stamp) information. Bias was set at –300V.](image)

Fig. 8 shows the Pole Zero Cancellation test results. The undershoot after the event pulse is normally produced in these type of circuits. The pole zero cancellation circuit eliminates the undershoot and allows for faster counting at higher rates.

![Fig. 8. a) Pole zero cancellation circuit on the RENA-3 chip is turned off and b) Pole zero cancellation is turned on.](image)

RENA-3 chip is used to take data simultaneously from all the channels of the 32 pixel 1x1 mm² pitch CdZnTe detector shown in Fig. 9. The detectors are fabricated by eV Products.

![Fig. 9. The CZT detector with 2x16 pixel array with 1x1 mm² pitch.](image)

Fig. 10 is showing ⁵⁷Co spectra taken from 32 channels simultaneously. The spectra from 16 channels are shown here. The differences between the spectra are due to the response of the CZT pixel detector and not due to the RENA-3 chip. There were a few channels, which did not show any spectra. These channels were the same channels, which did not produce data using other test methods or readout electronics.

**VII. CONCLUSION**

Initial results of tests on the RENA-3 chip have been quite encouraging. Full characterization of this chip is currently underway with an eye on performance parameters and functionalities that can find immediate use in instrument prototyping; aspects of the design requiring revision for the next version are also being determined. “Daughter” chip designs based on the versatile, multi-feature RENA-3 can be envisioned as custom readout solutions optimized for specific x-ray and gamma-ray spectroscopy applications.

**VIII. ACKNOWLEDGMENTS**

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IX. REFERENCES


Fig. 10: Co-57 spectra taken simultaneously using all the pixels of the 32 pixel CdZnTe detector. Sixteen of the spectra taken are shown here. The differences between the spectra are due to the response of the pixels of the CdZnTe pixel detector and not due to the RENA-3 chip.